

# DSP Pro Development Board Stratix II 2S180 Edition

## Rev 01

Revision History		
Date	Change Description	Rev
8/18/05	Created schematic and changed the component from the 2S60 on the DSP board to the 2S180 on this Pro version of the board	01

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Title

DSP Pro Stratix II 2S180 (Maine Pro)

Size

A

Document Number

P06-10217-01

Rev

01

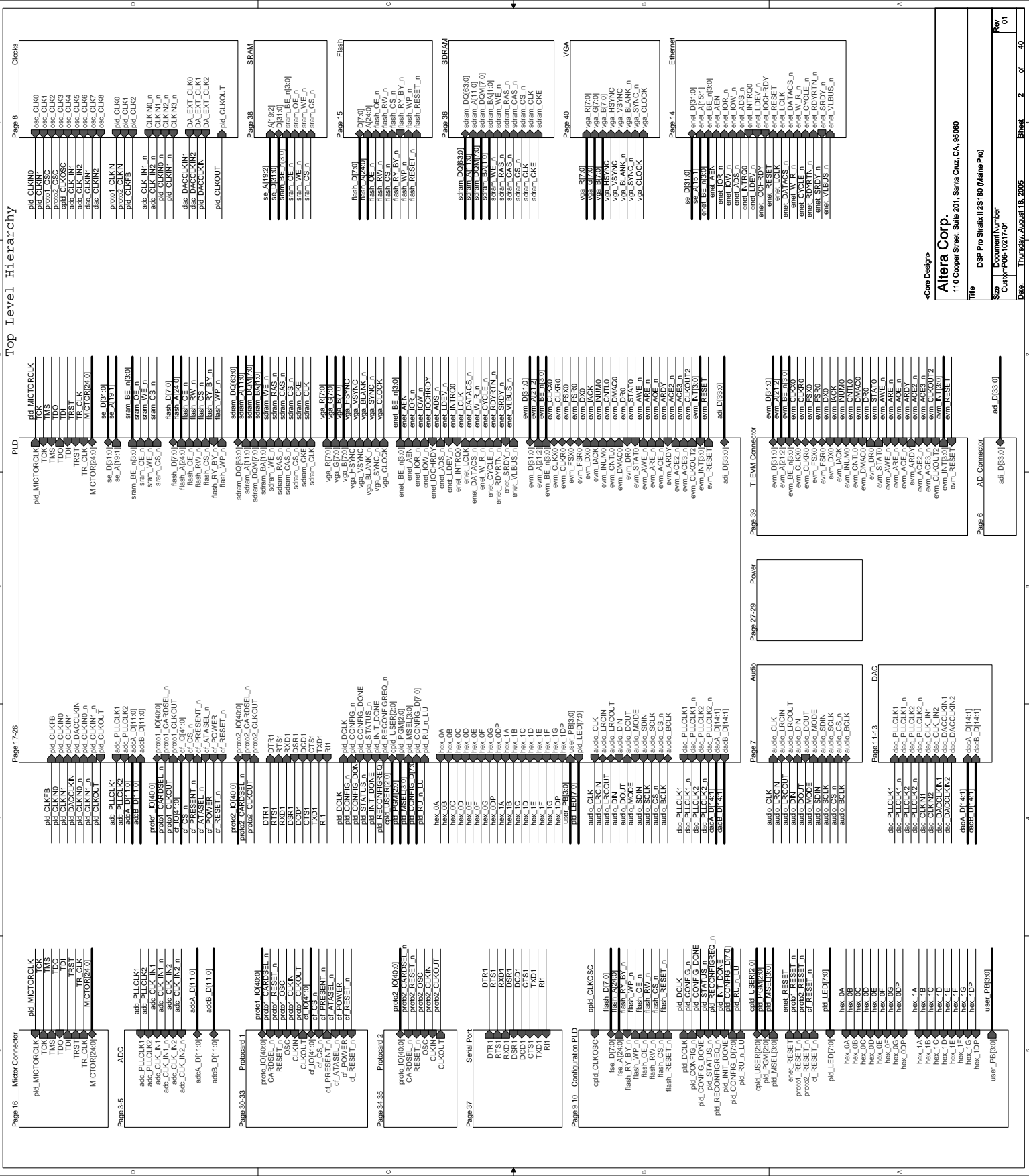
Date:

Thursday, August 18, 2005

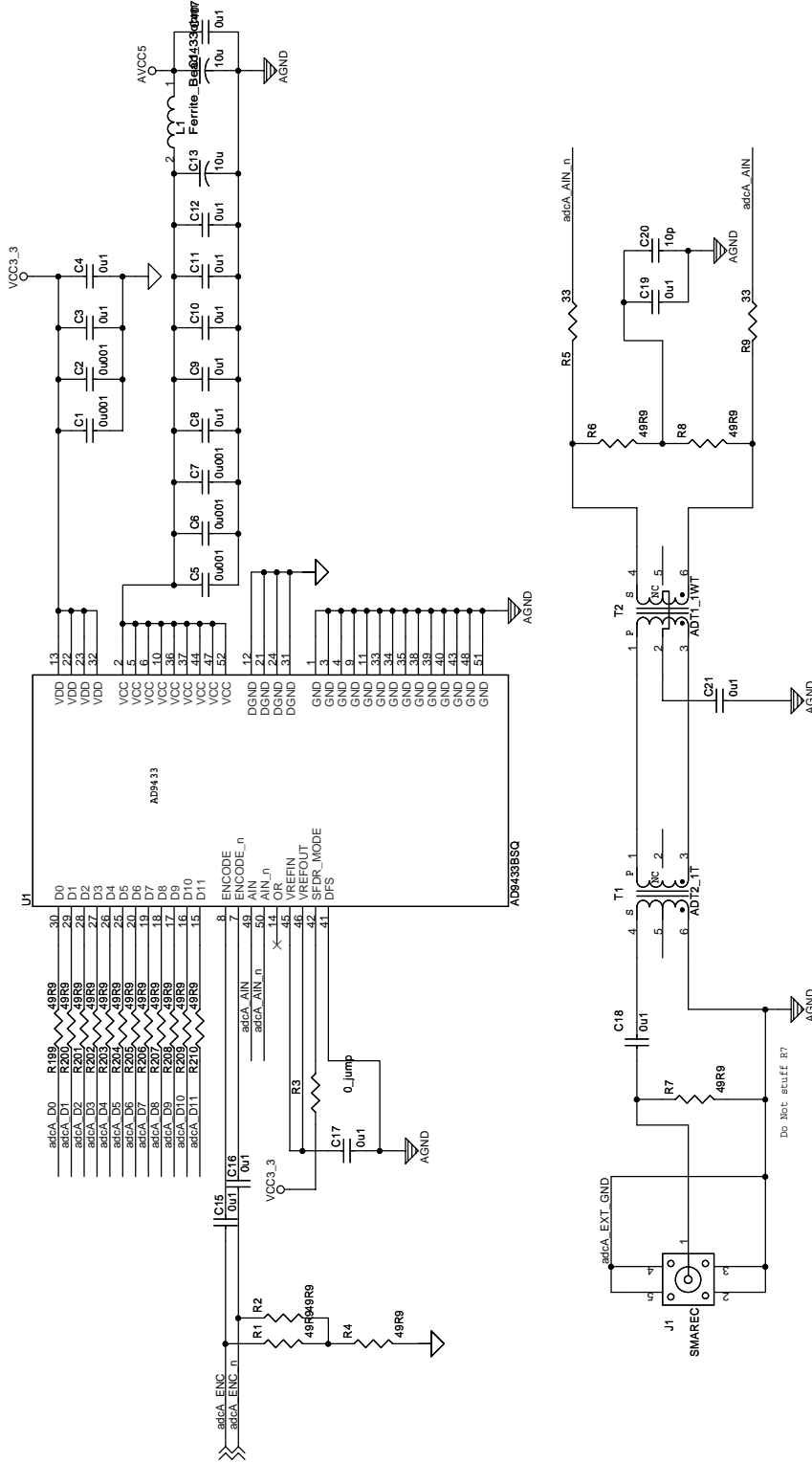
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Top Level Hierarchy



adca\_d11.01



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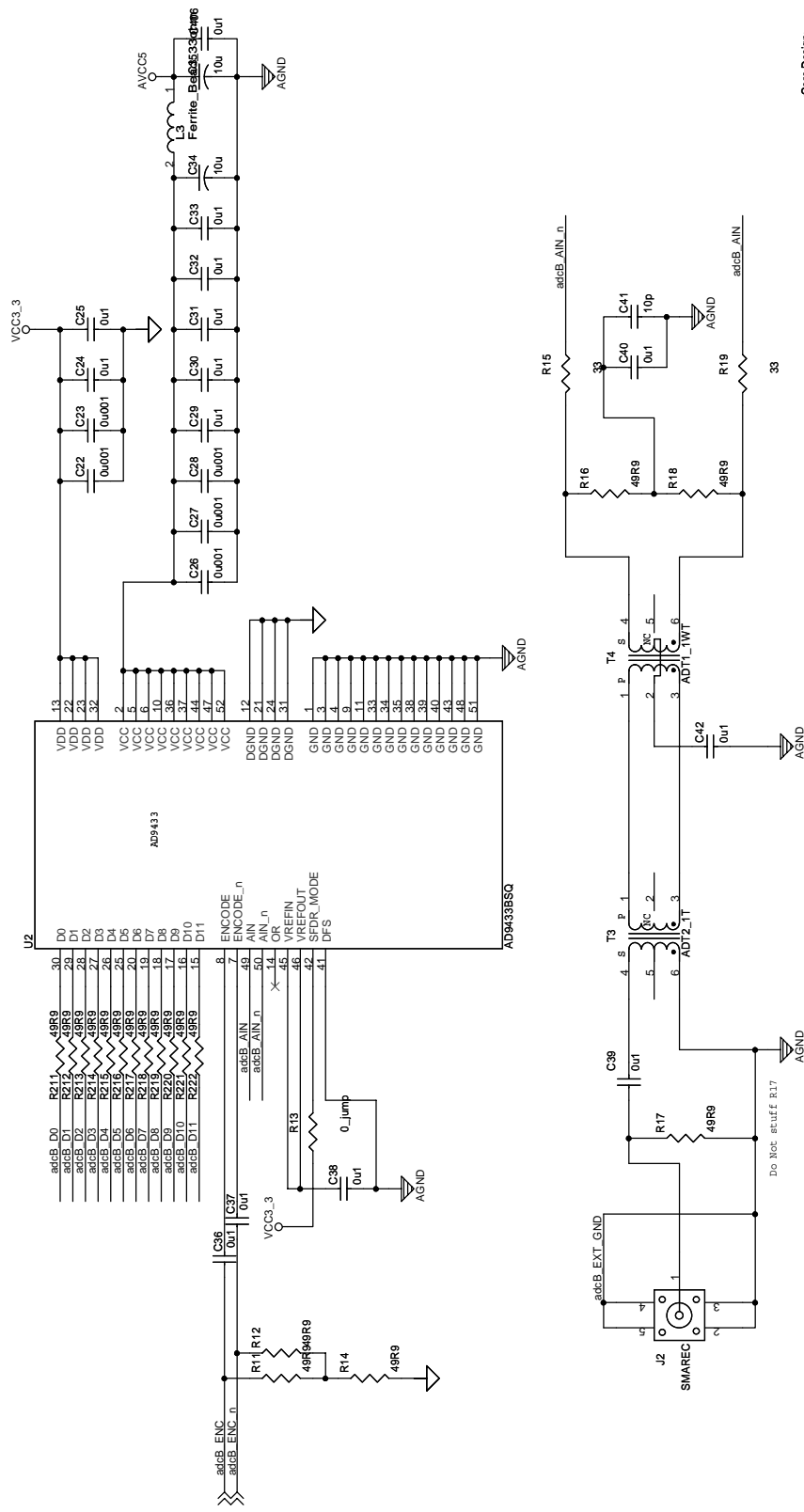
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adcB\_D11101



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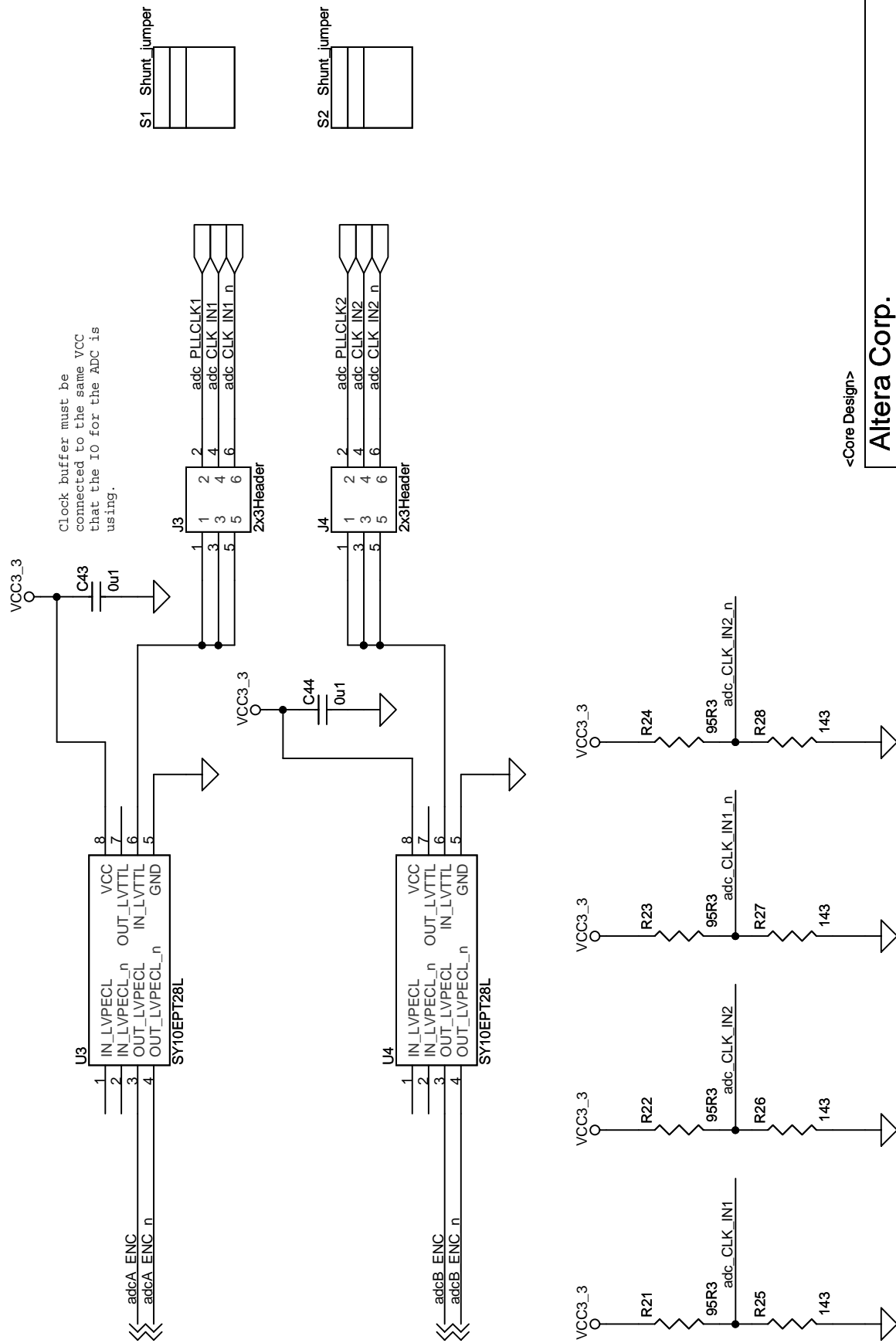
Size B Document Number P06-10217-01

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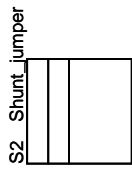
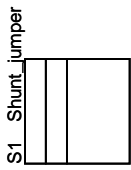
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# ADC Clock Selection



Clock buffer must be connected to the same VCC that the IO for the ADC is using.



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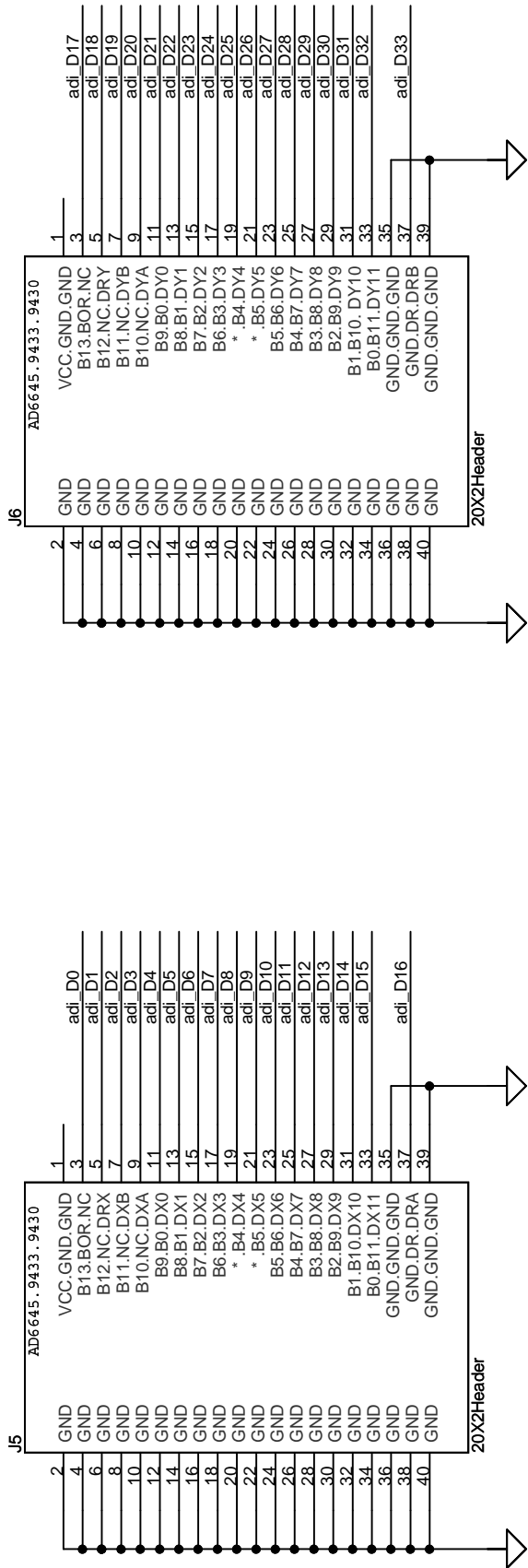
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# ADI Connector

adi\_D133:01



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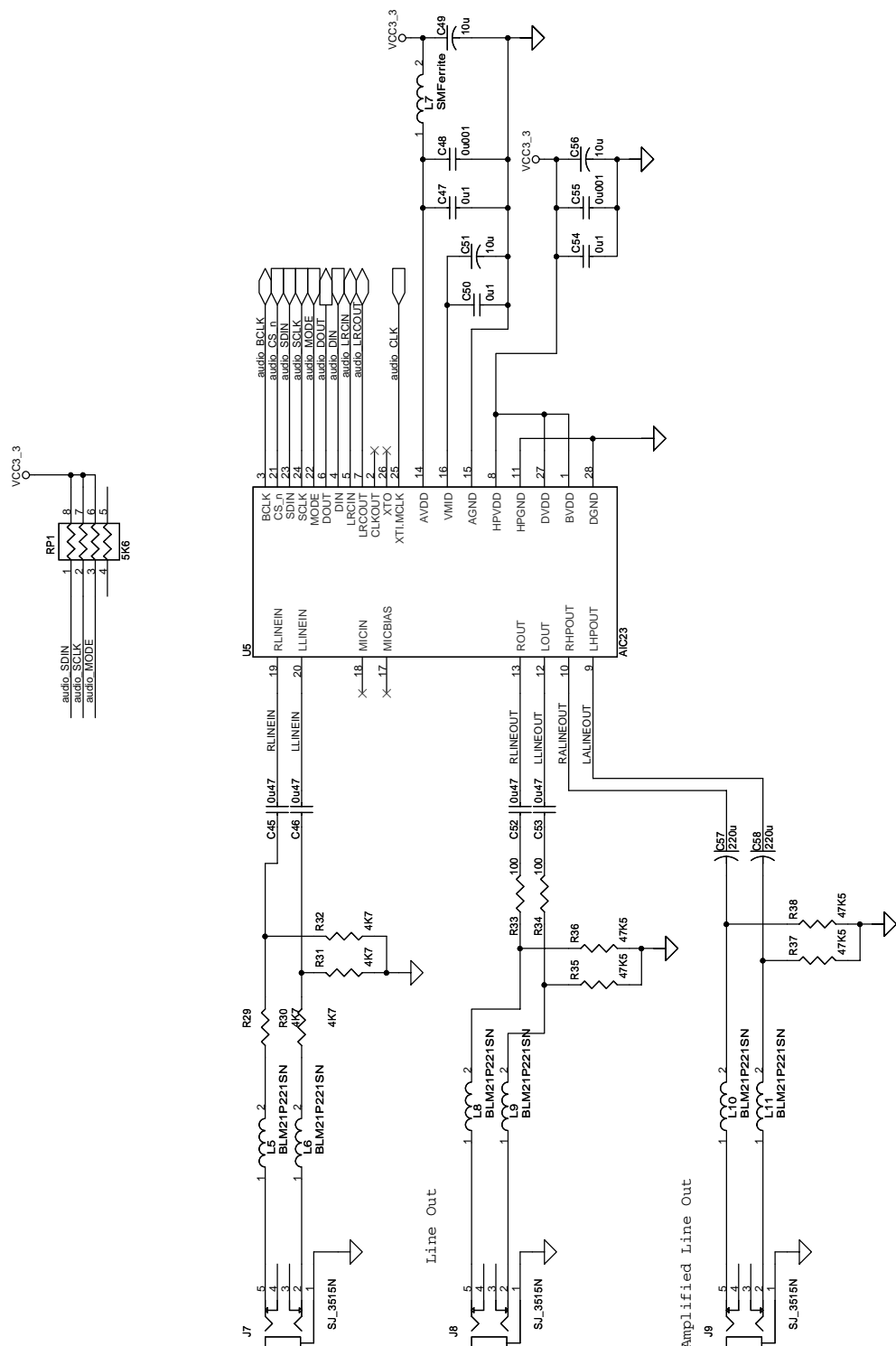
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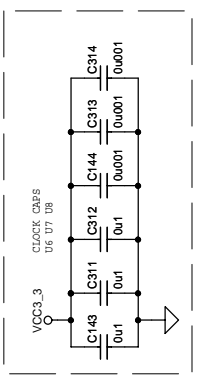
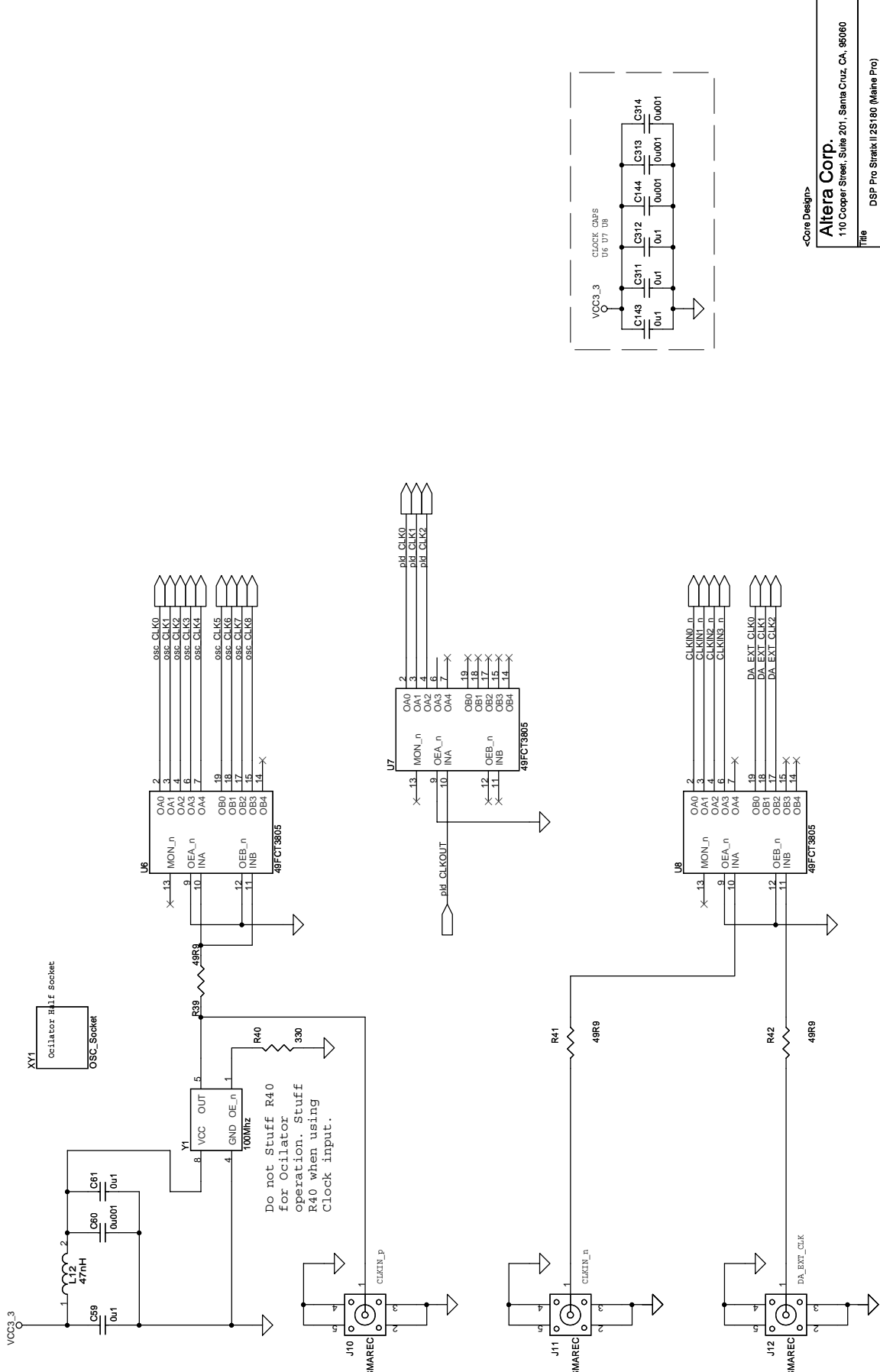
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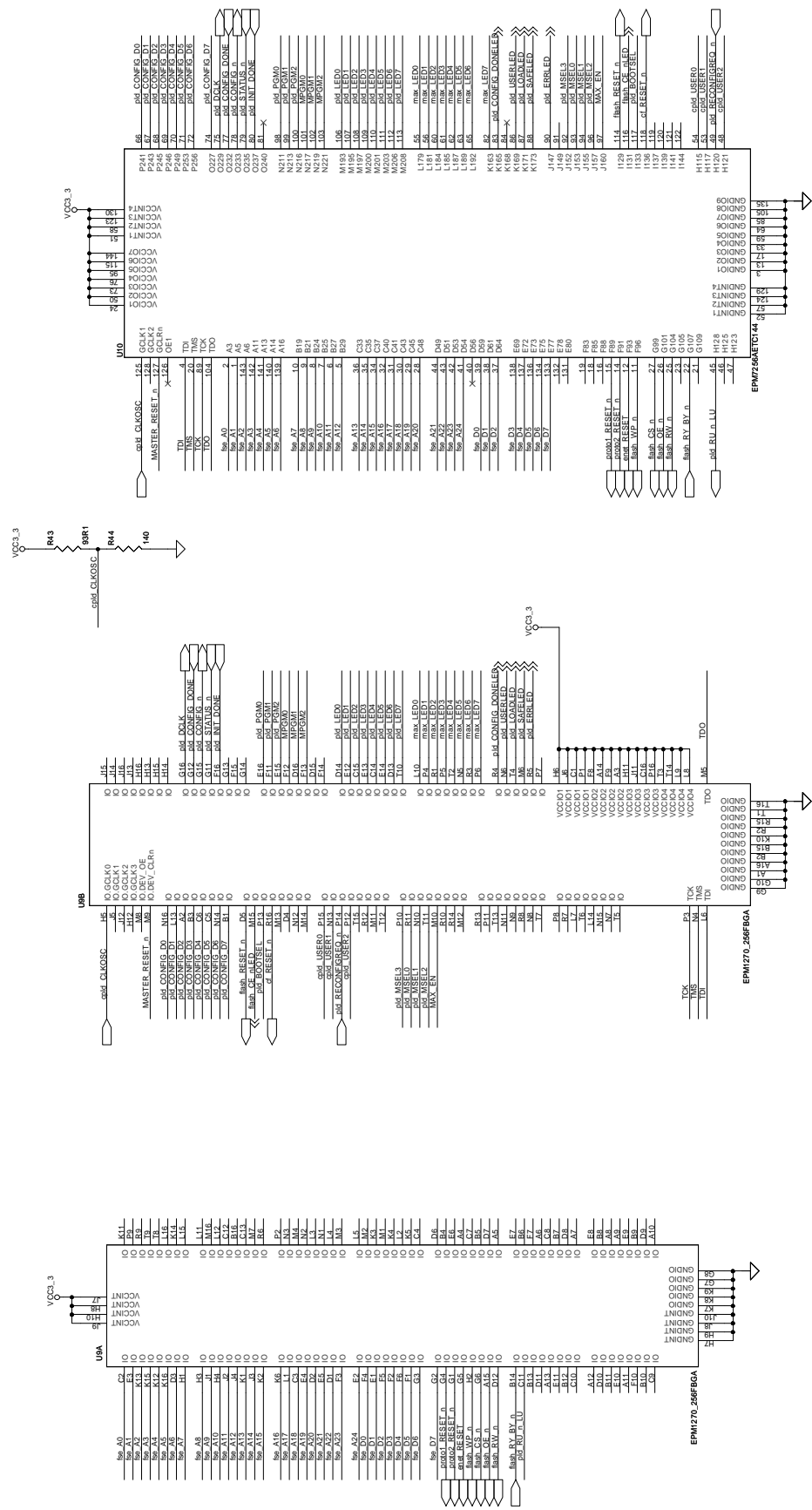
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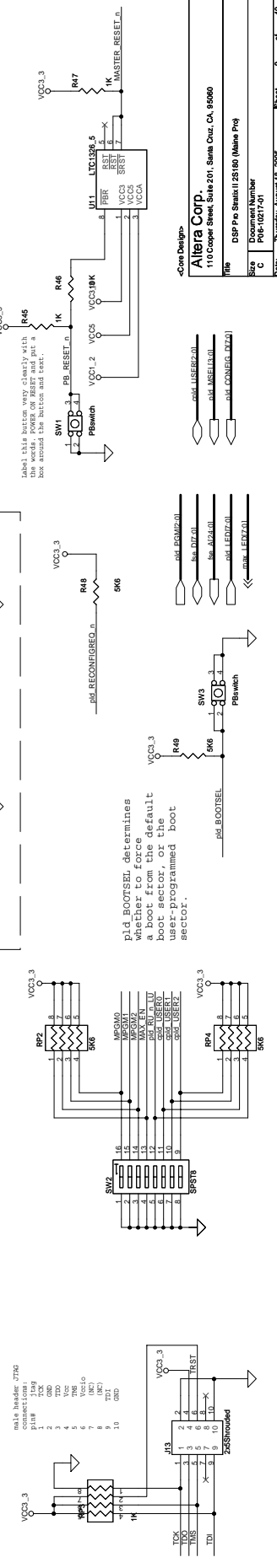
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Configuration PLD

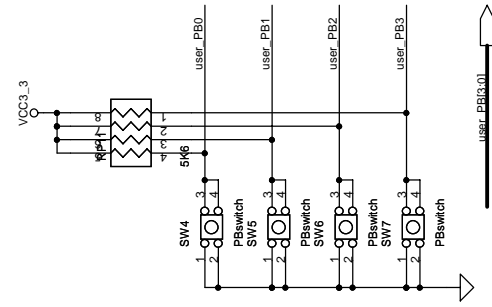
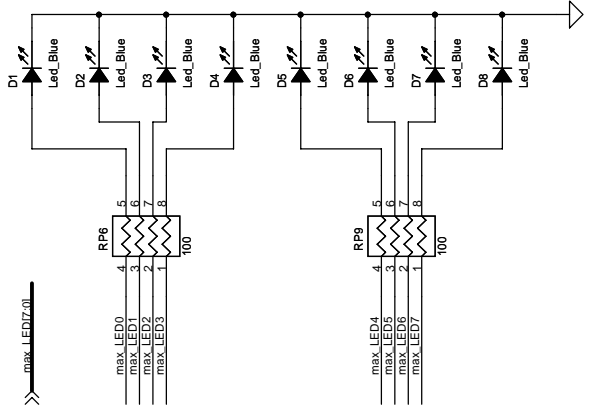
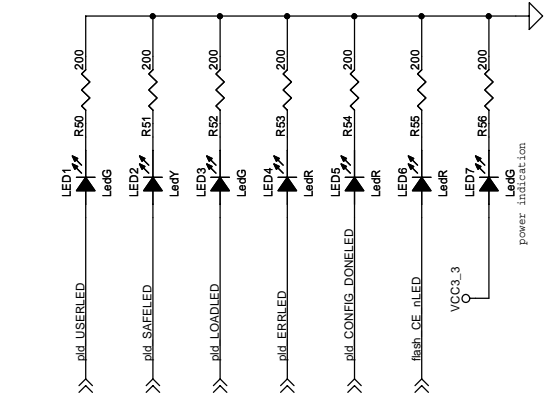


Configuration PLD



Note: This button may assembly with the words: POWER ON RESET and pin 4 box around the button and text.

pld BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.



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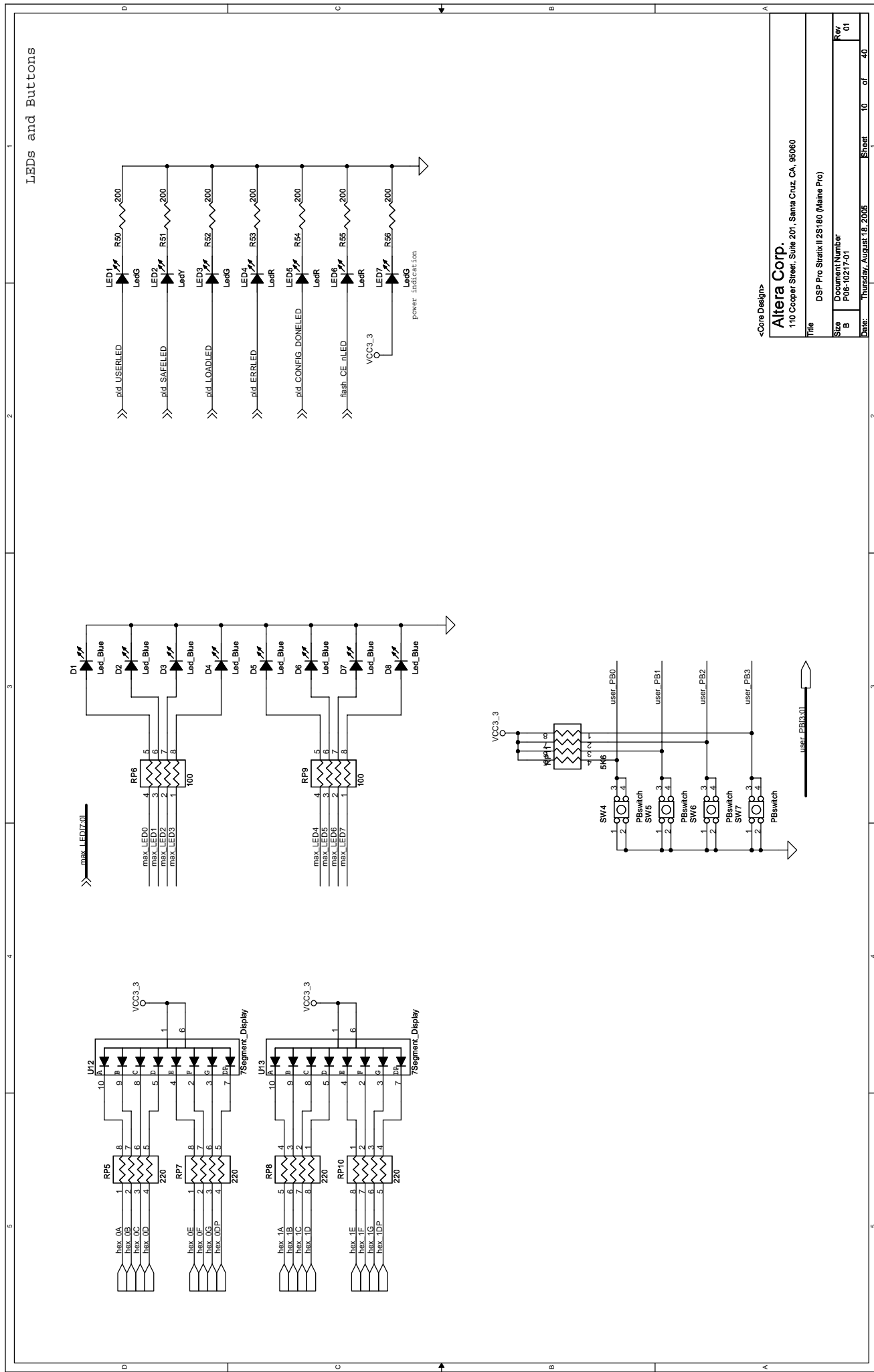
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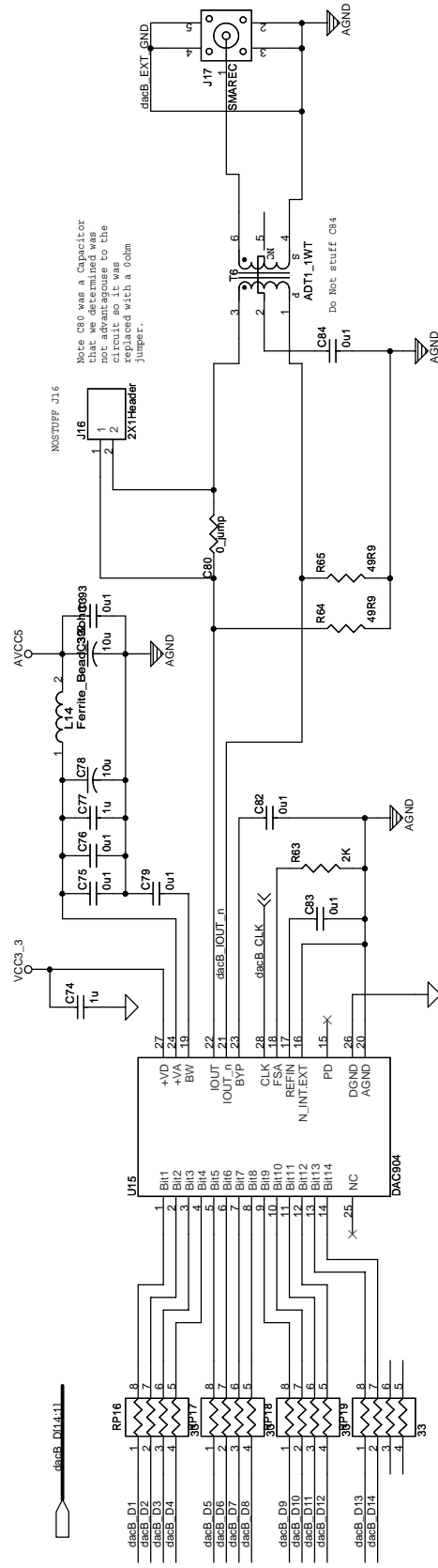
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Title DSP Fio Strata II 2S180 (Maine Fio)

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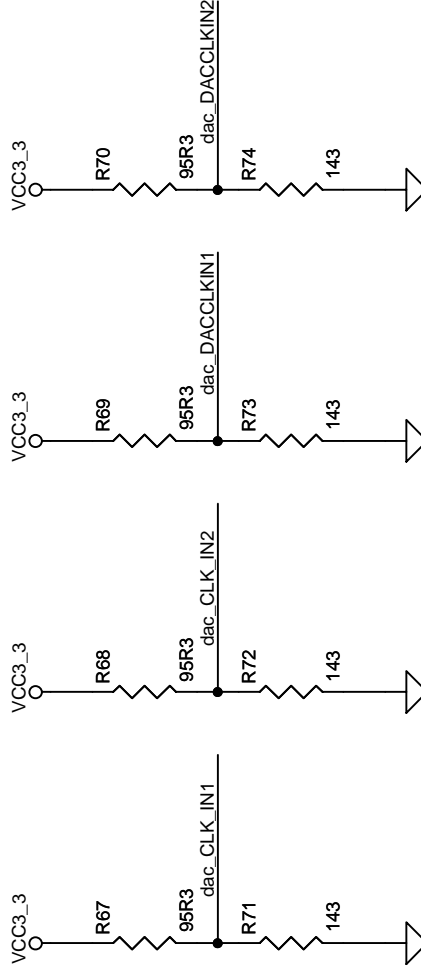
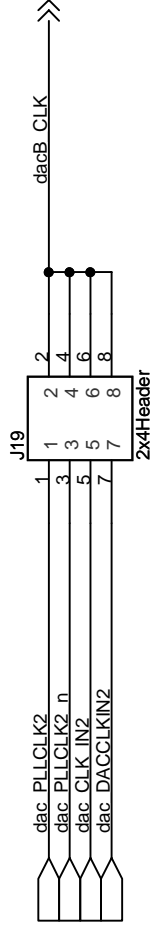
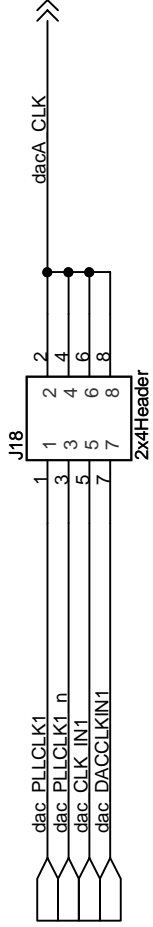
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# DAC Clock Jumper

S3 Shunt jumper



S4 Shunt jumper



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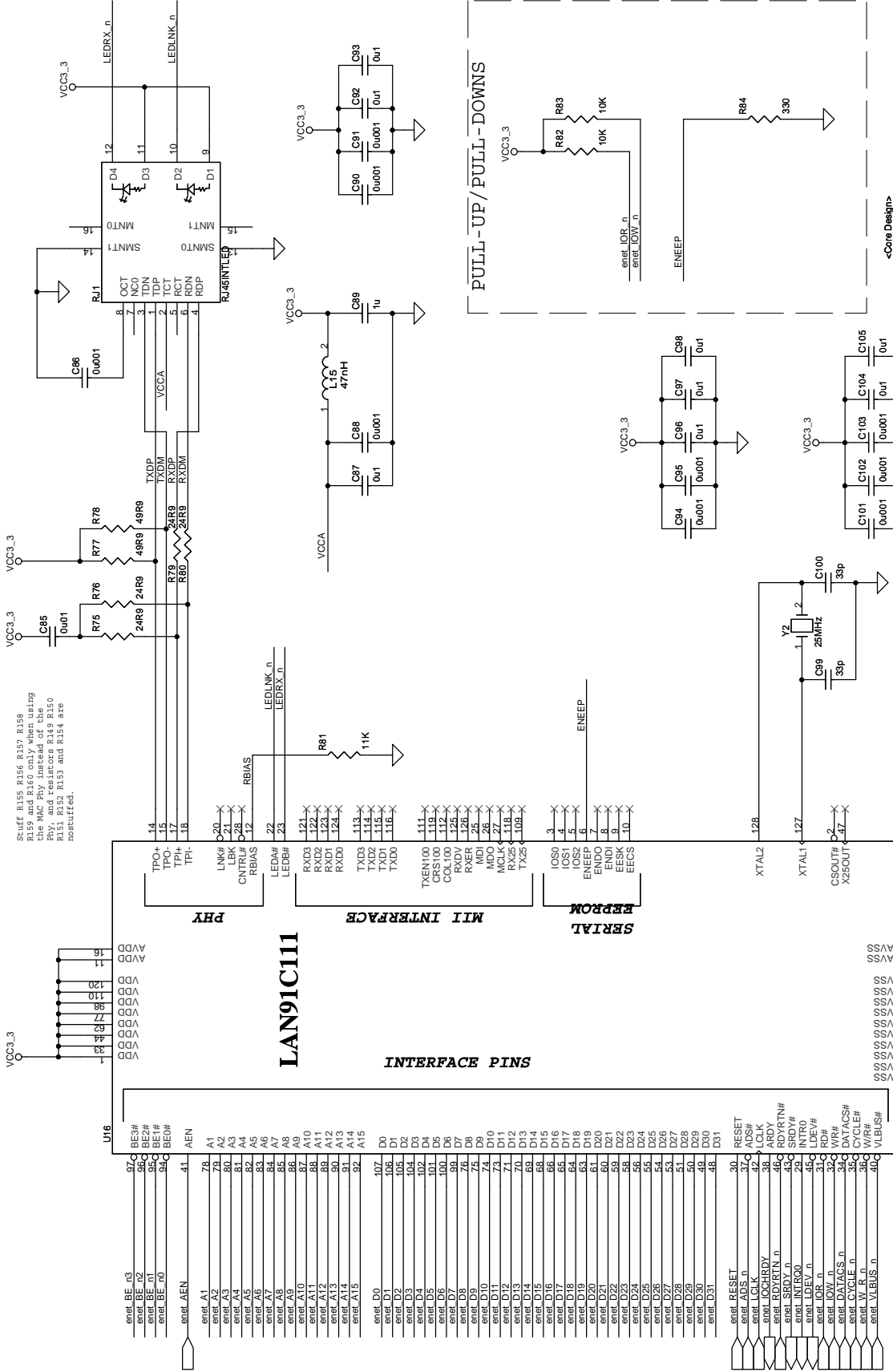
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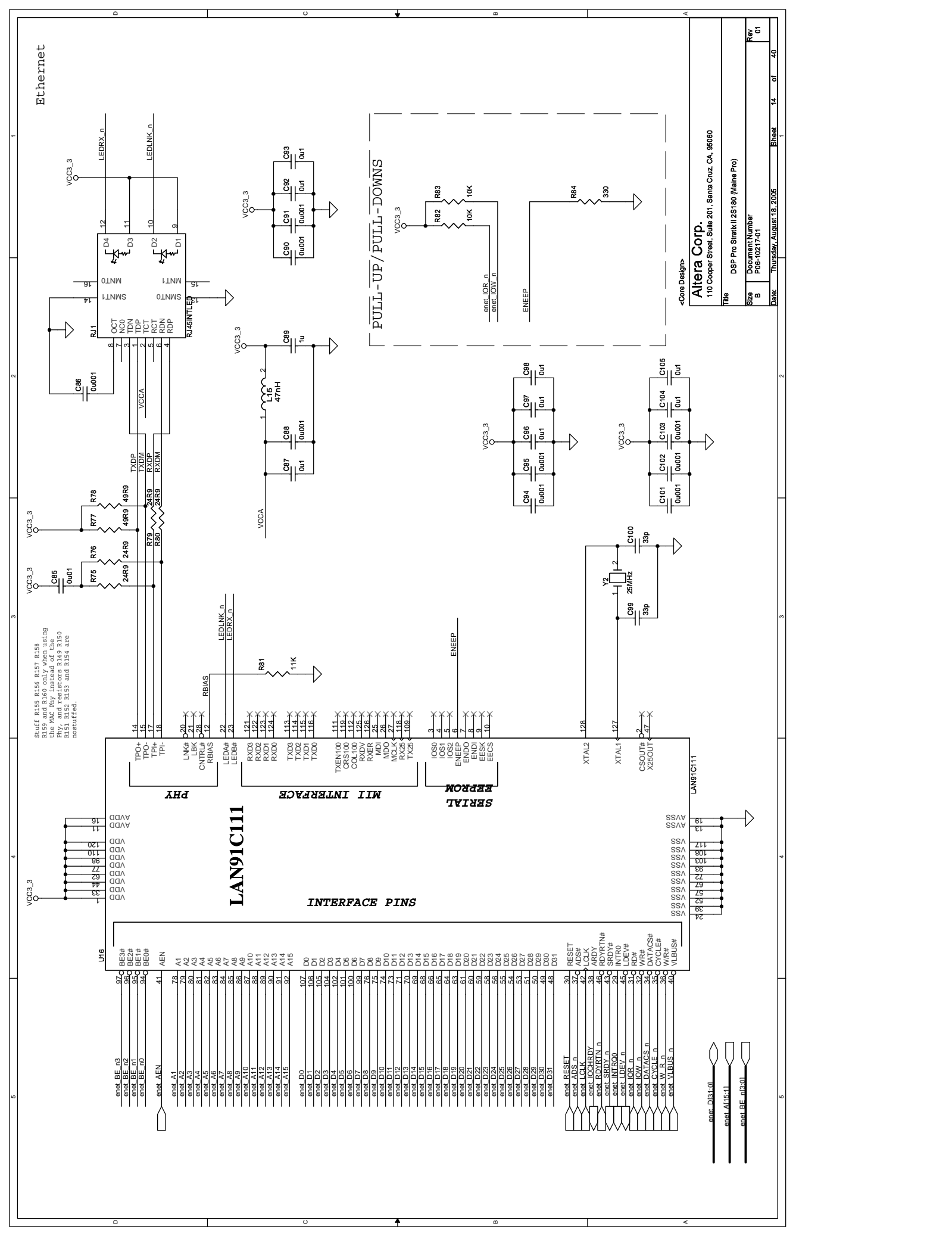
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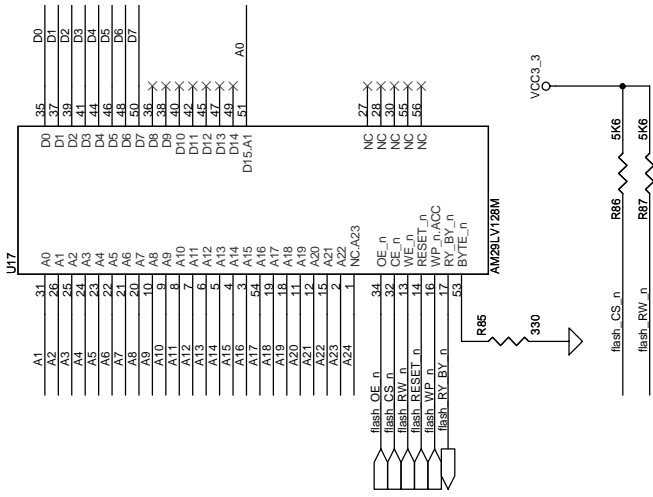
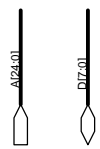
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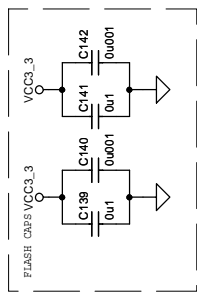
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Shift R155, R156, R157, R158, R159 and R160 only when using the MAC Phy instead of the PHY, and resistors R149, R150, R151, R152, R153 and R154 are unpopulated.





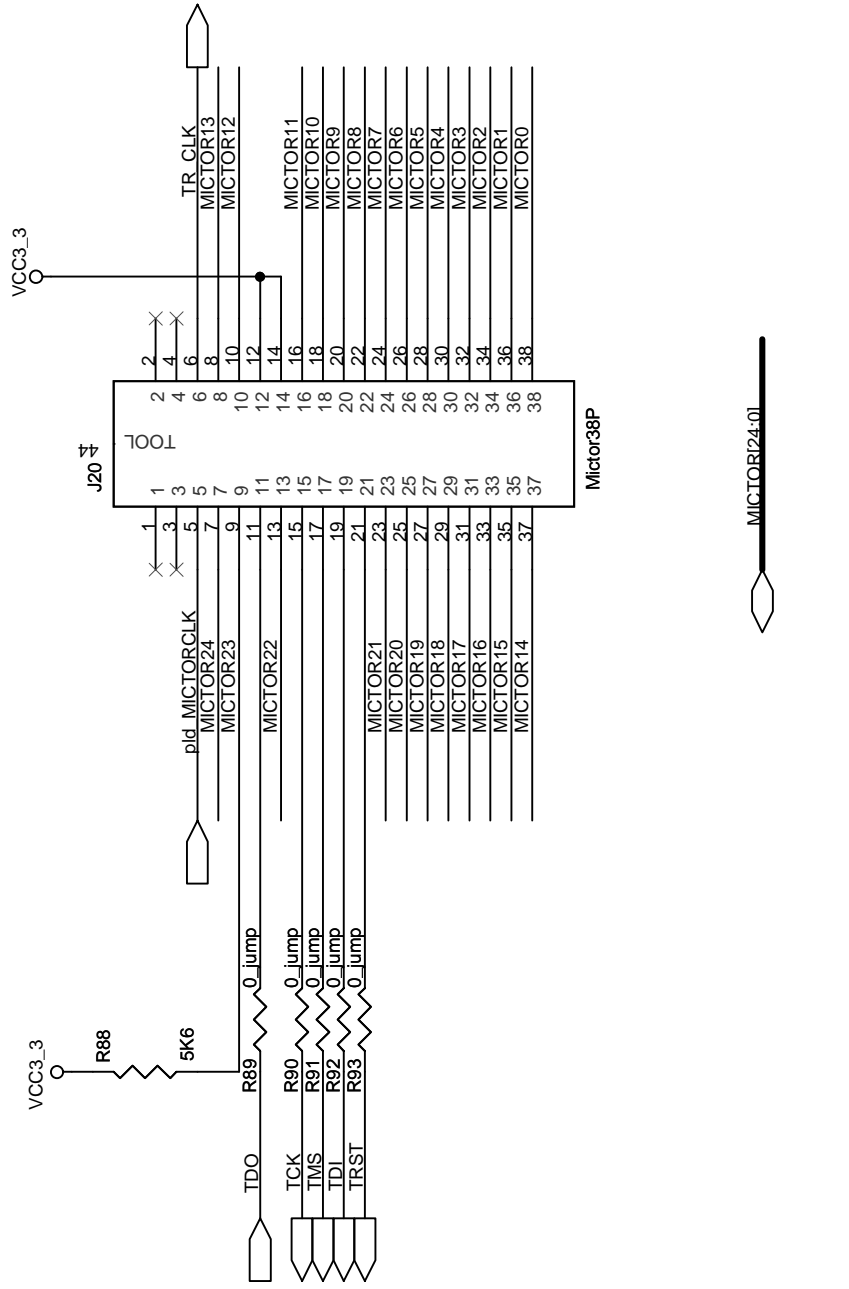
Flash chip is 16M x 8 for 16Mbytes of flash



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# Mictor Connector



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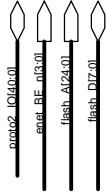
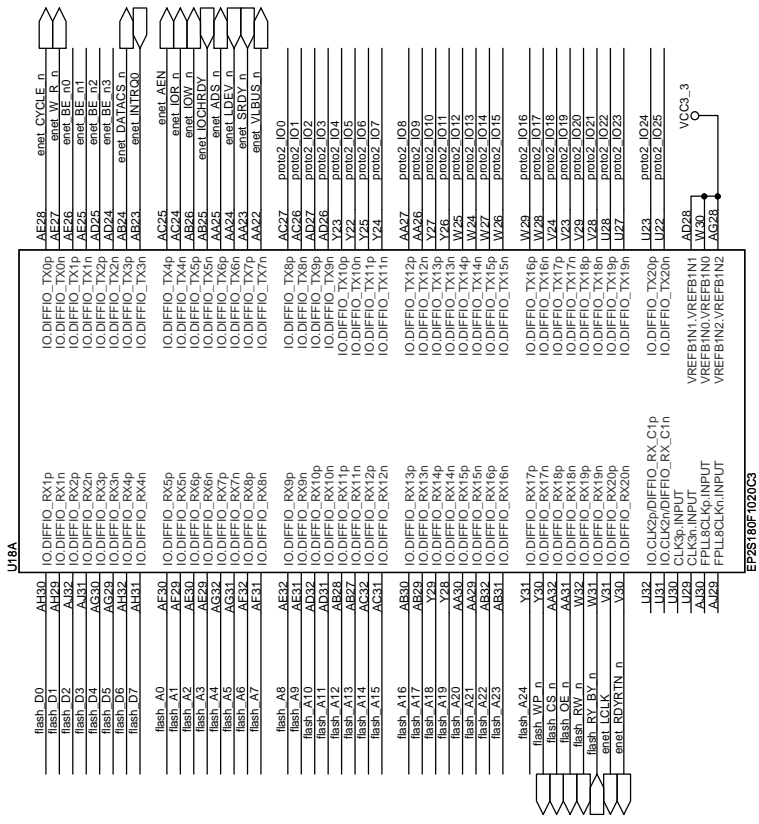
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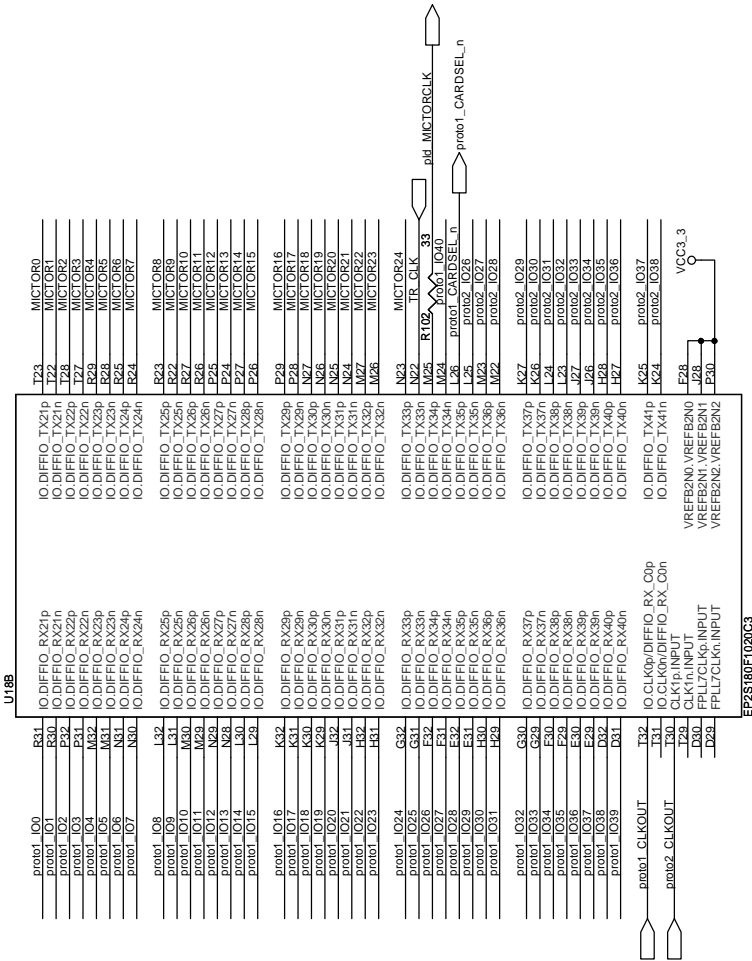
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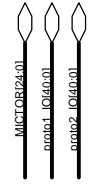
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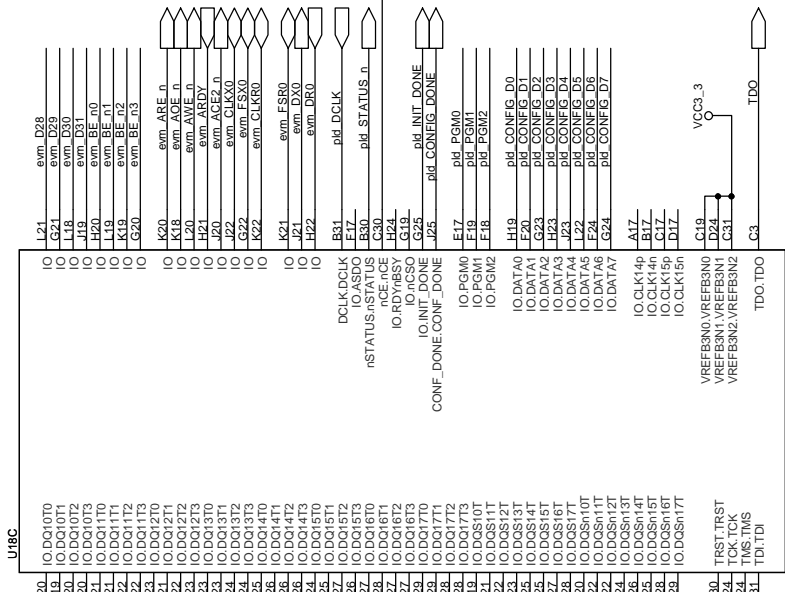
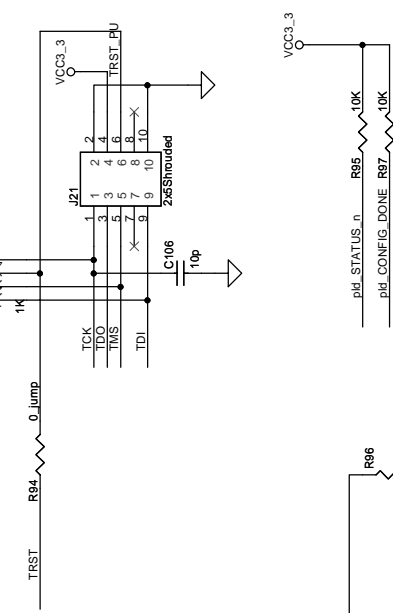


EP2S180F1020C3

PLD Bank 3

- male header JTAG
- connectors
- pin#
- 1 GND
- 2 TCK
- 3 VCC3\_3
- 4 TRST
- 5 VDD
- 6 VDD
- 7 VDD
- 8 VDD
- 9 TDI
- 10 GND

Do not stuff R94



EP2K100C3

- evm\_AIP212
- evm\_DI1401
- evm\_BE\_n1301
- pd\_PGM201
- pd\_CONFIG\_D1201

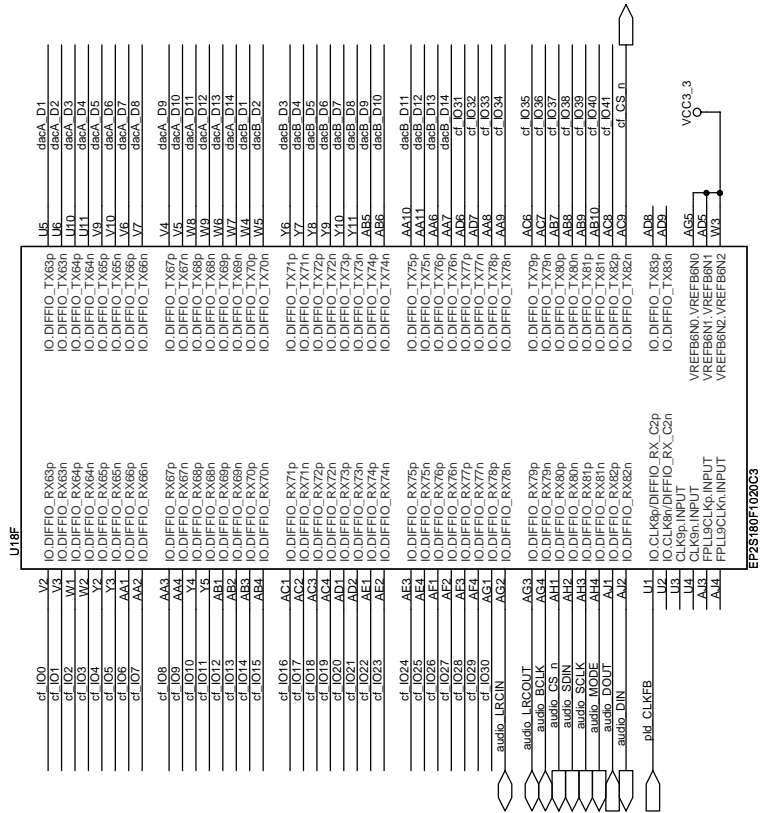
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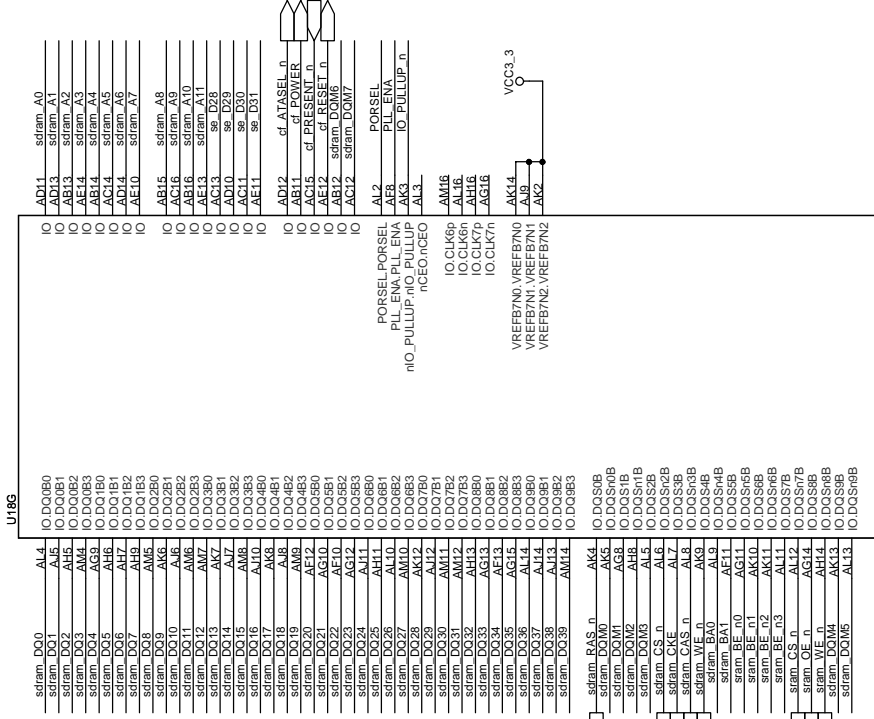






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- sa\_D14:0
- sfram\_DQ163:0
- sfram\_A11:0
- sfram\_BA1:0
- sfram\_DQM7:0
- sram\_BE\_n[3:0]

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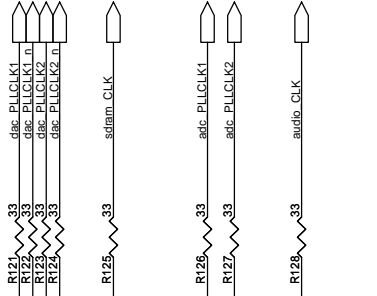




U18J

- L28 NC
- ADA NC
- AE28 NC
- G28 NC
- M27 NC
- AC29 NC
- AC30 NC
- AD3 NC
- J28 NC
- L27 NC
- W26 NC
- M10 NC
- M11 NC
- F2 NC
- M13 NC
- M14 NC
- W22 NC
- AE27 NC
- AD30 NC
- AE3 NC
- AE6 NC
- AE5 NC
- AE8 NC
- AE14 NC
- G19 NC
- G21 NC
- AG26 NC
- H1 NC
- F26 NC
- G8 NC
- H8 NC
- H9 NC
- H8 NC

- IO.PLL5\_OUT0p
- IO.PLL5\_OUT0n
- IO.PLL5\_OUT1p
- IO.PLL5\_OUT1n
- IO.PLL5\_FBpOUT2p
- IO.PLL5\_FBnOUT2n
- IO.PLL6\_OUT0p
- IO.PLL6\_OUT0n
- IO.PLL6\_OUT1p
- IO.PLL6\_OUT1n
- IO.PLL6\_FBpOUT2p
- IO.PLL6\_FBnOUT2n
- IO.PLL11\_OUT0p
- IO.PLL11\_OUT0n
- IO.PLL11\_OUT1p
- IO.PLL11\_OUT1n
- IO.PLL11\_FBpOUT2p
- IO.PLL11\_FBnOUT2n
- IO.PLL12\_OUT0p
- IO.PLL12\_OUT0n
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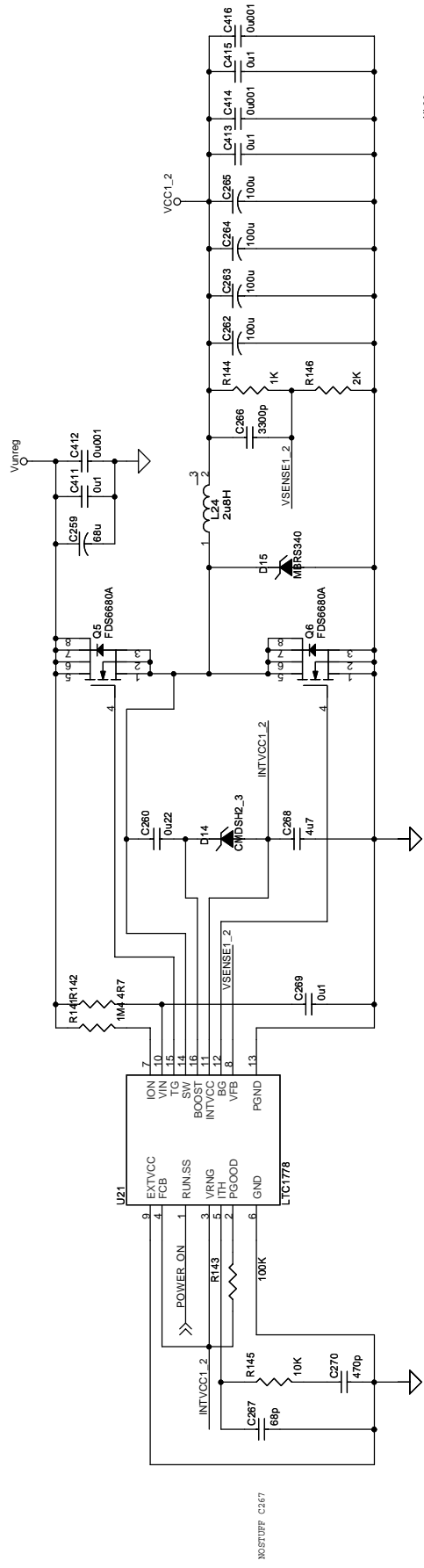
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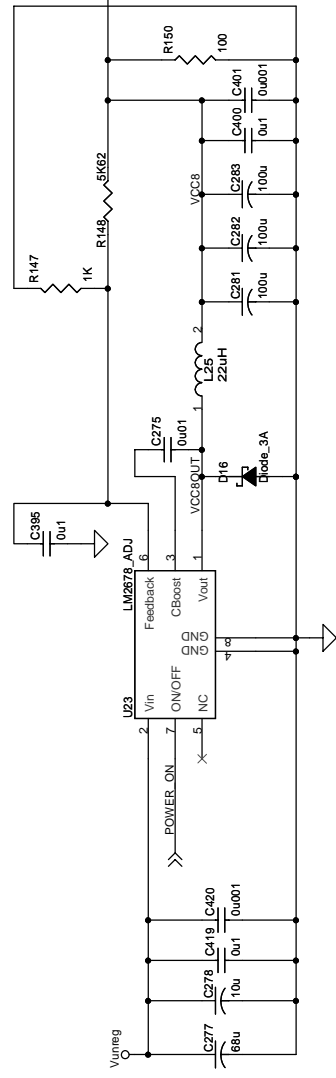
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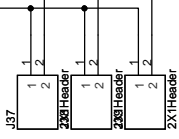
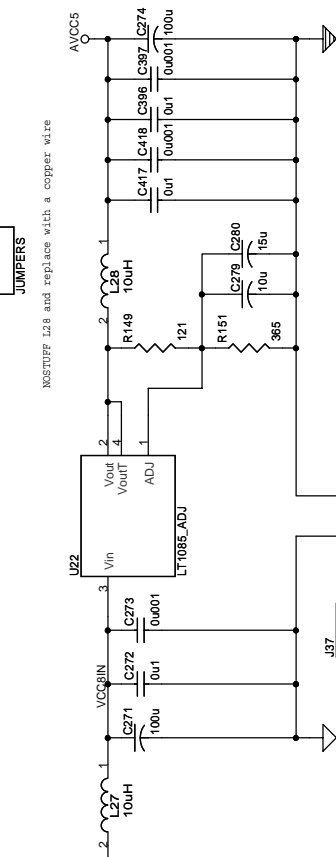


JUMPERS

WSTUFF L28 and replace with a copper wire



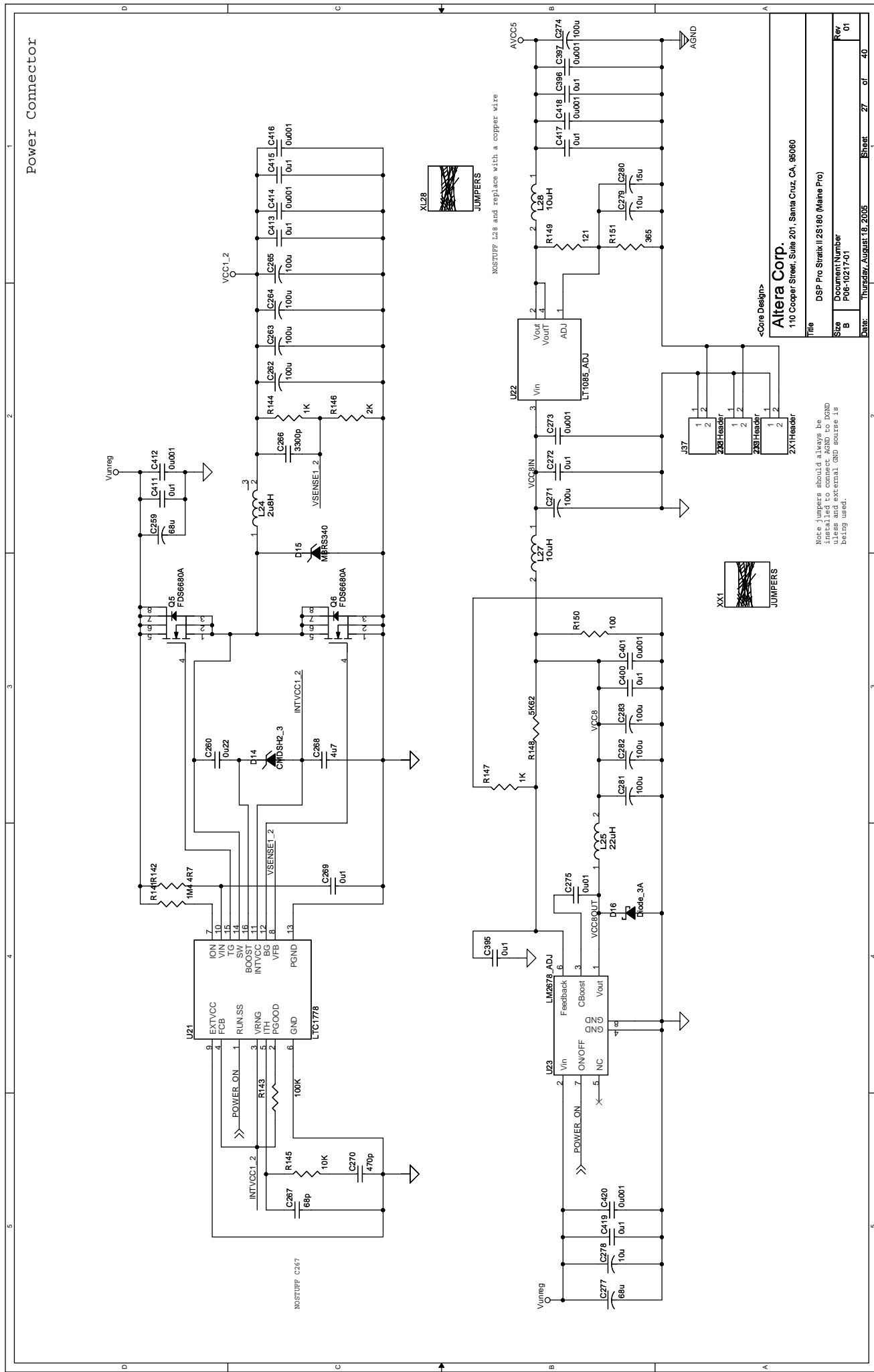
JUMPERS



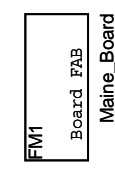
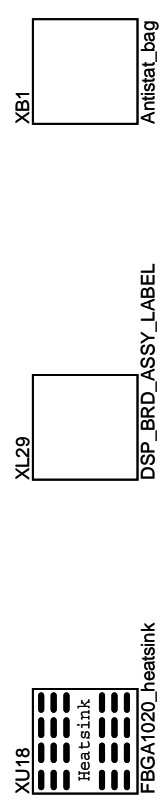
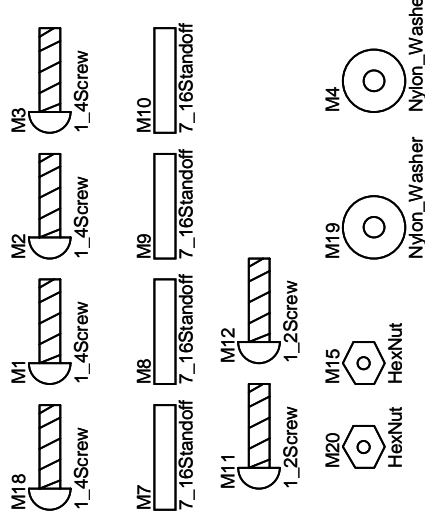
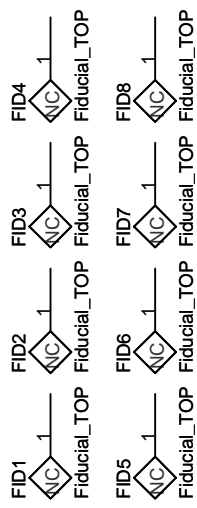
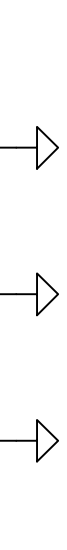
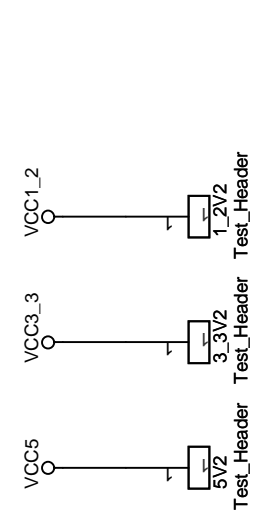
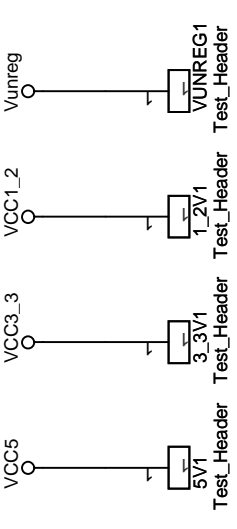
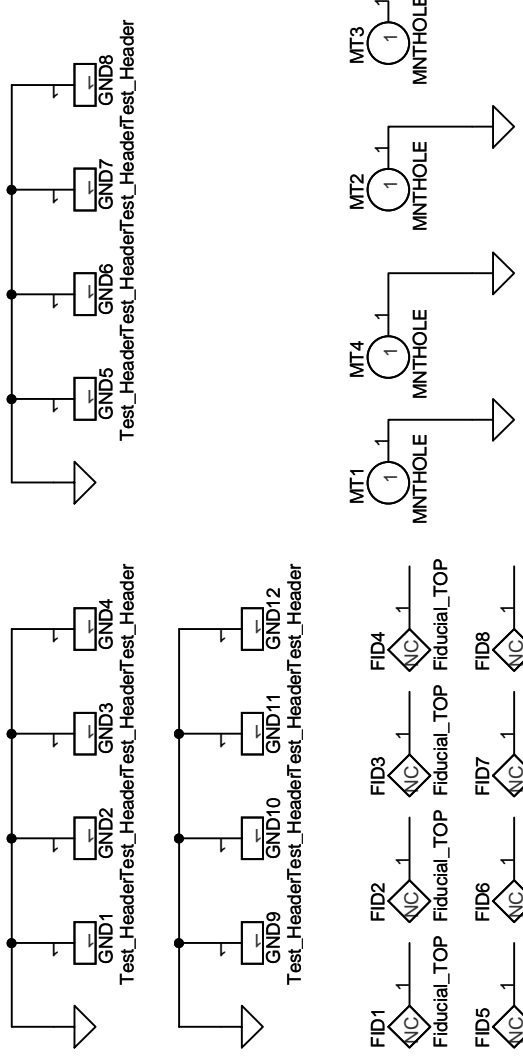
Note jumpers should always be installed to connect AGND to PGND unless and external GND source is being used.

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# Reset and Test headers



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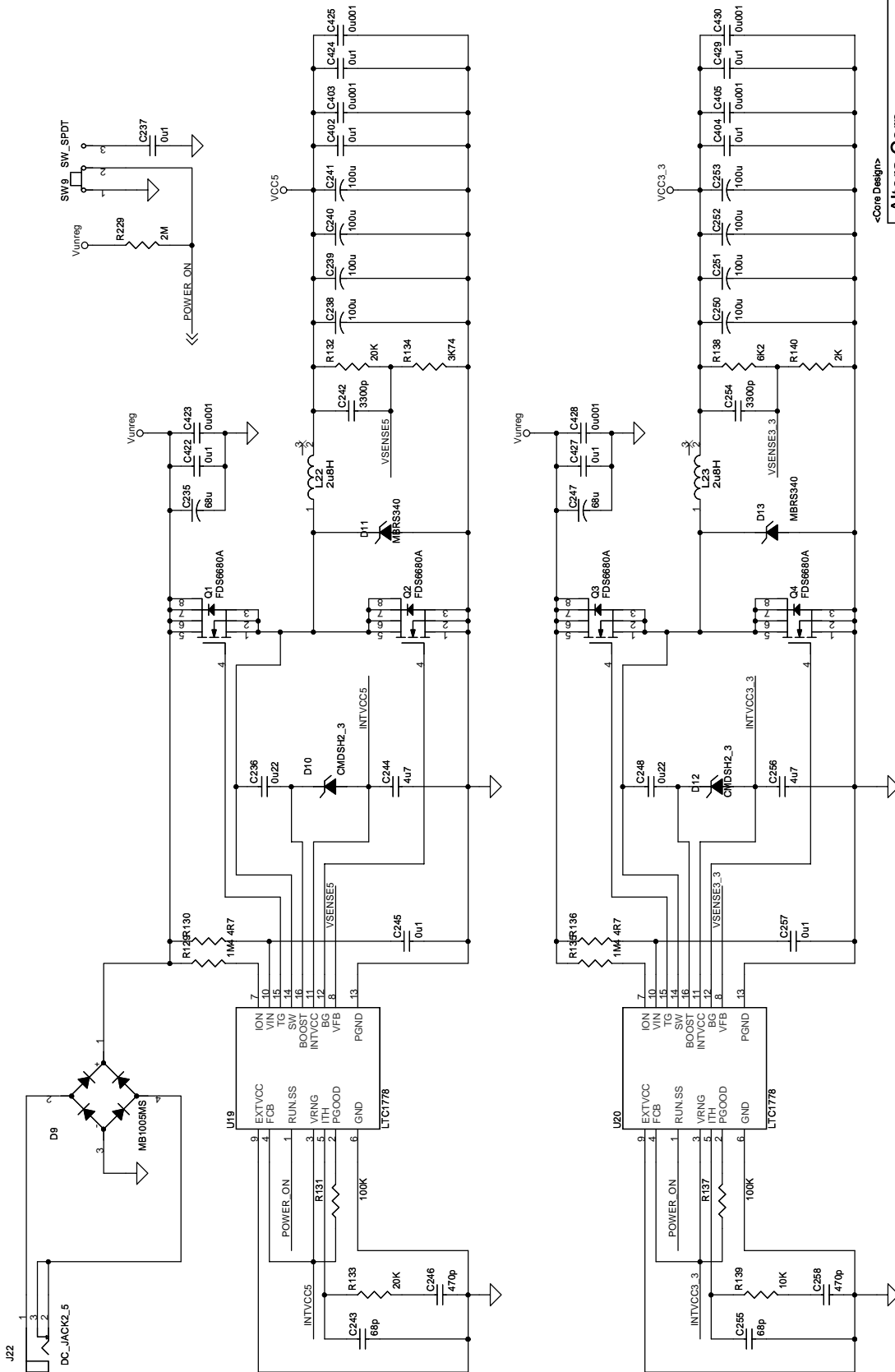
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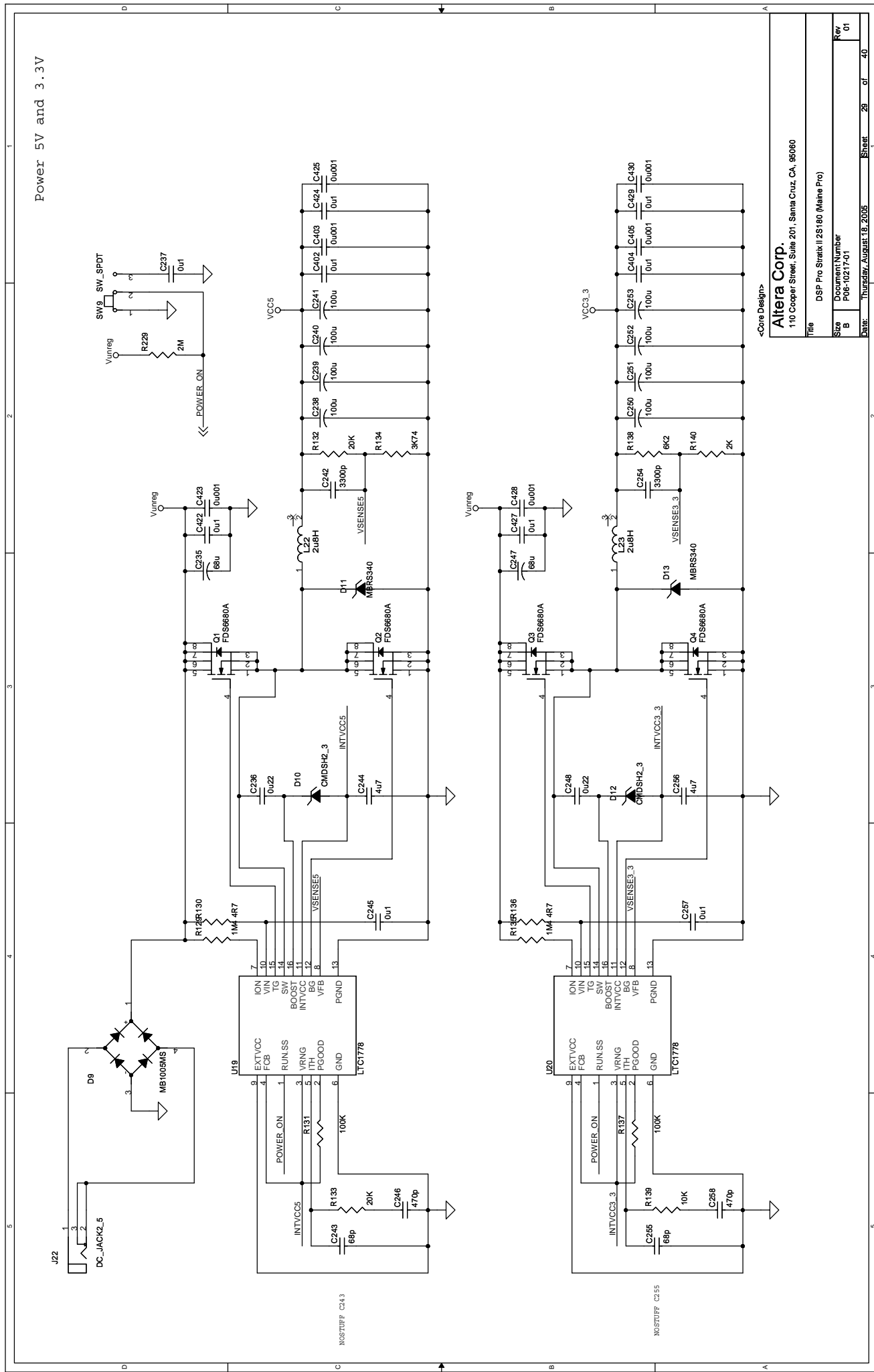
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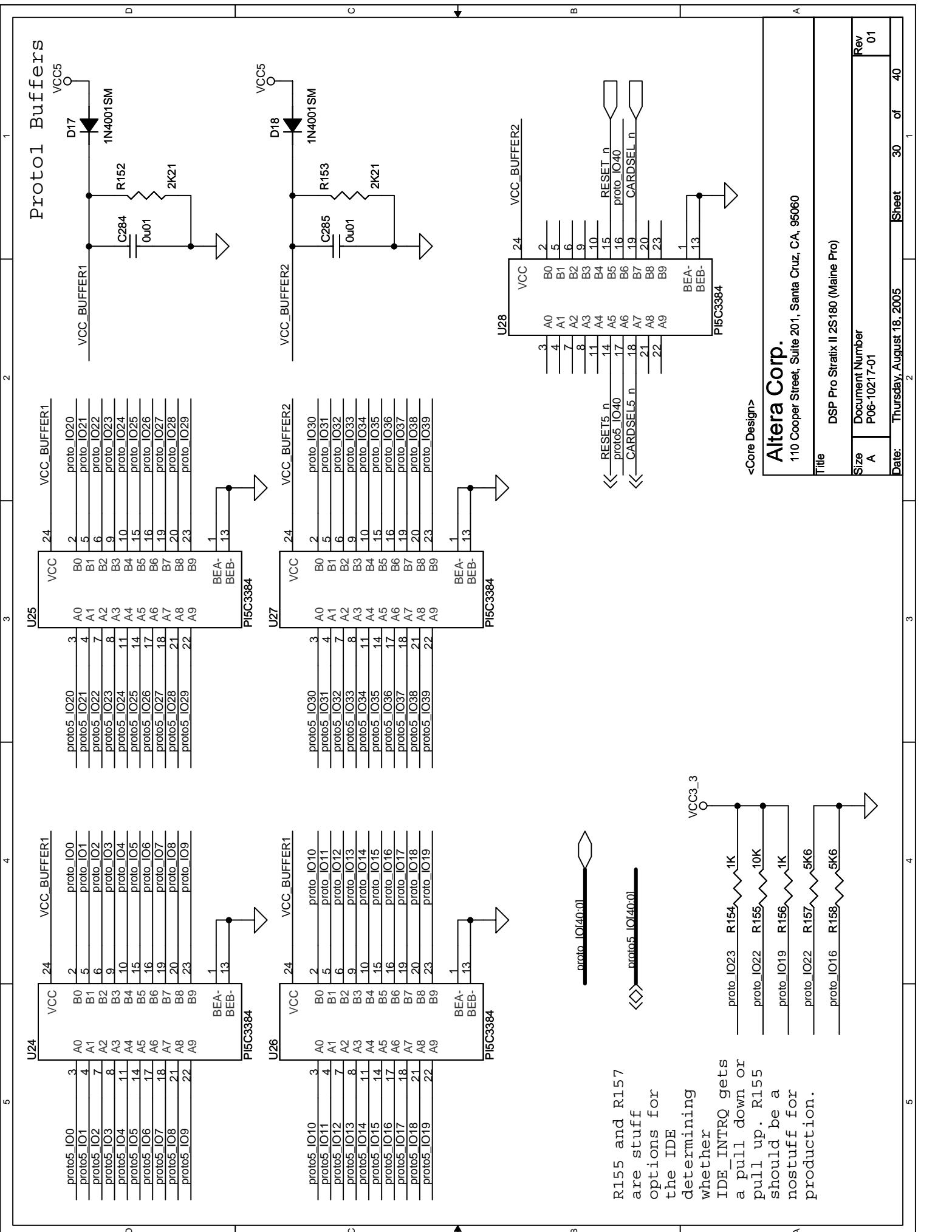
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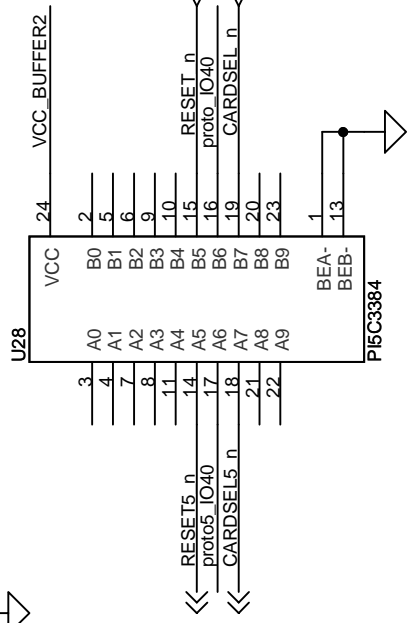
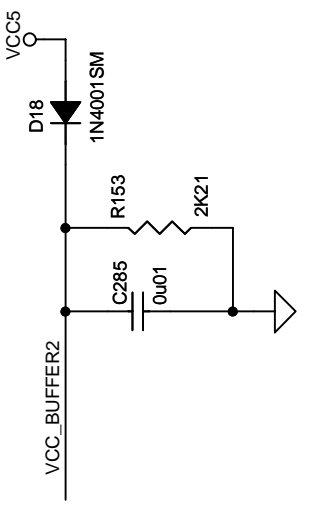
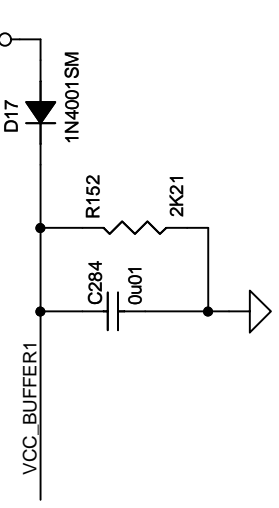
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Proto1 Buffers



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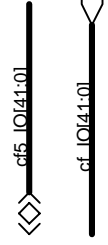
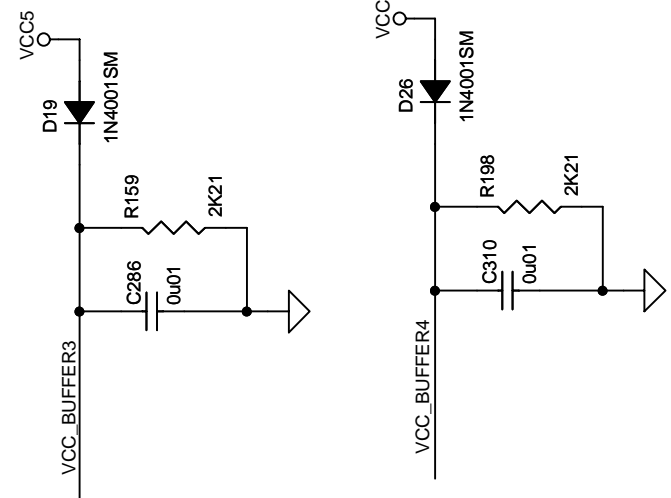
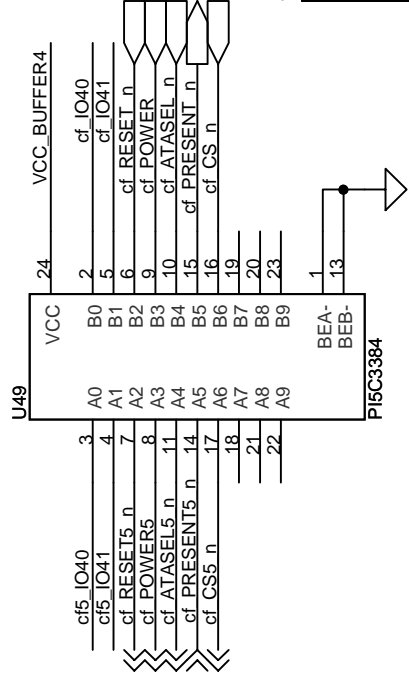
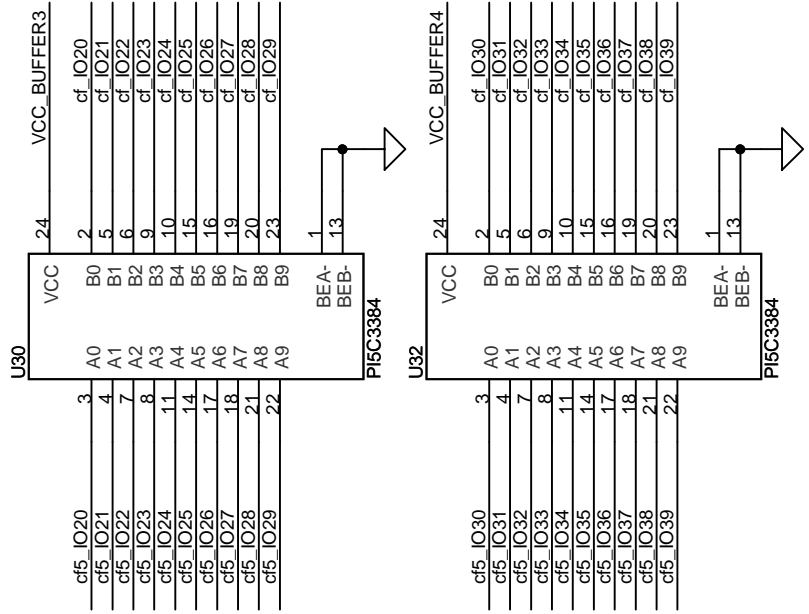
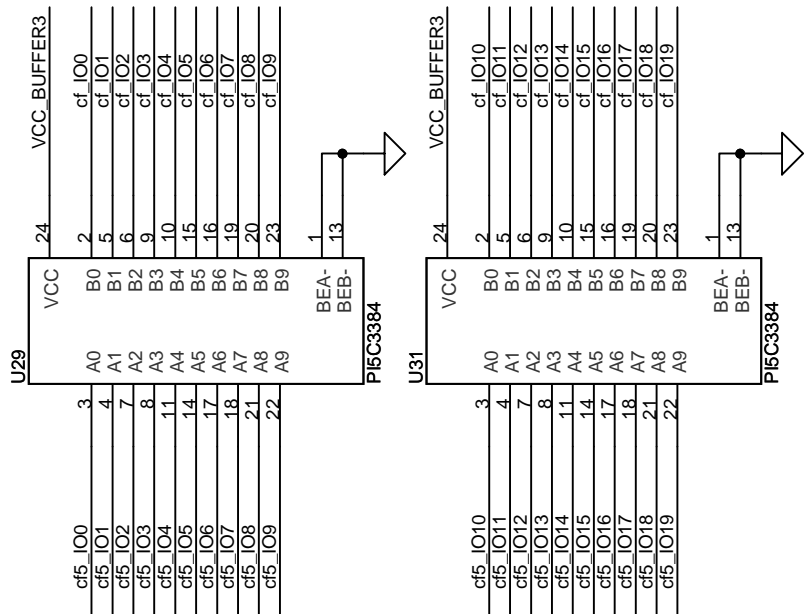
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R155 and R157 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.

# Proto1 Buffers



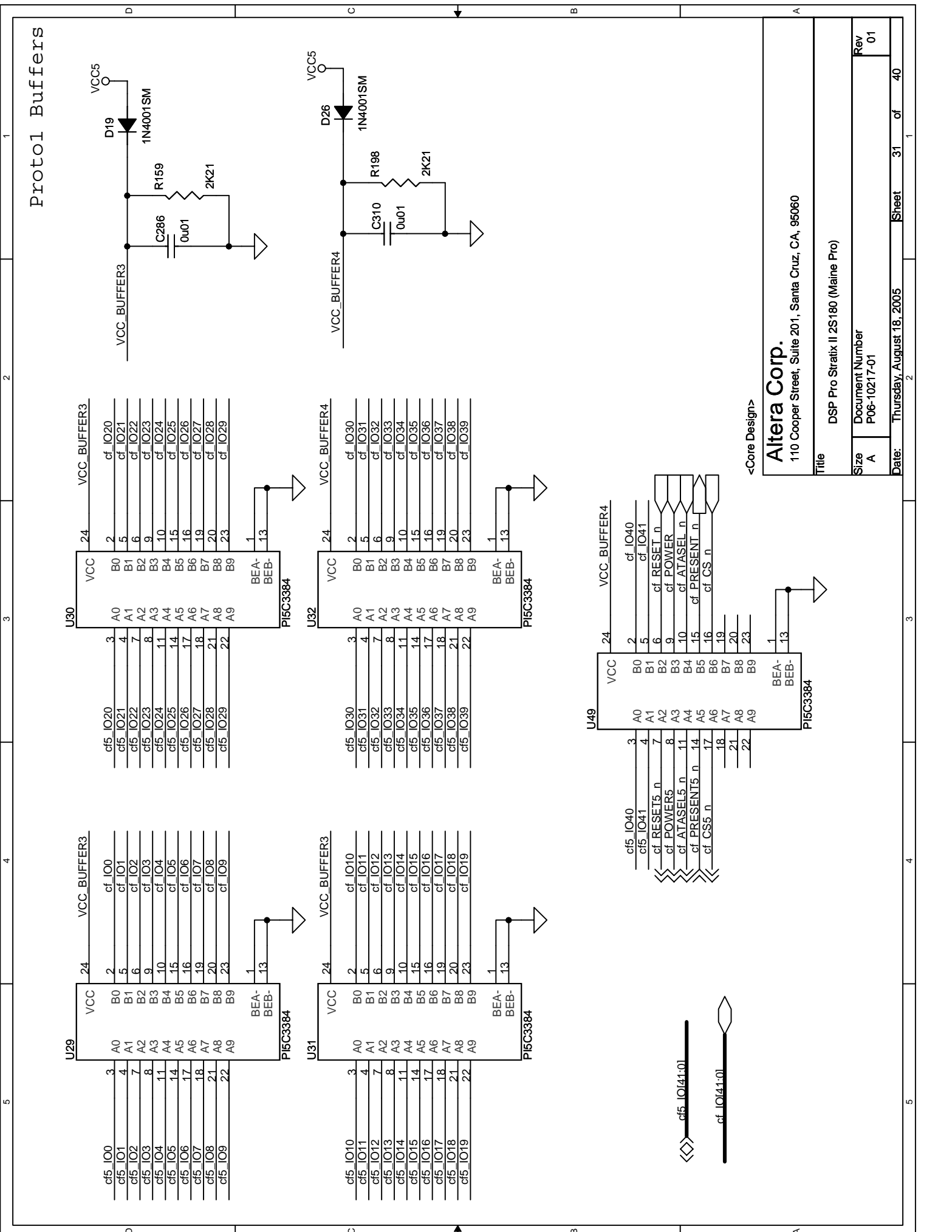
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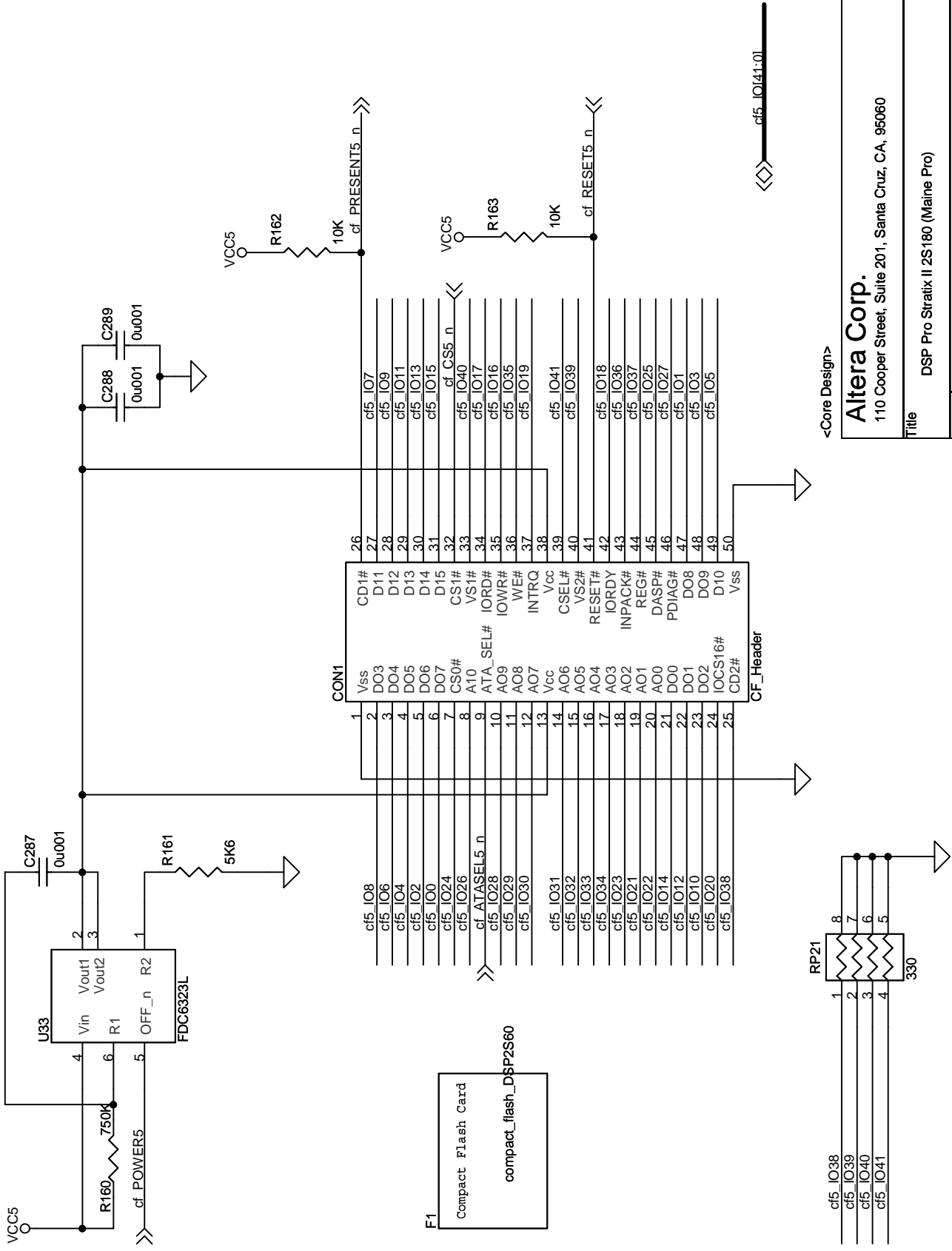
Title: DSP Pro Stratix II 2S180 (Maine Pro)

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# Compact Flash Socket



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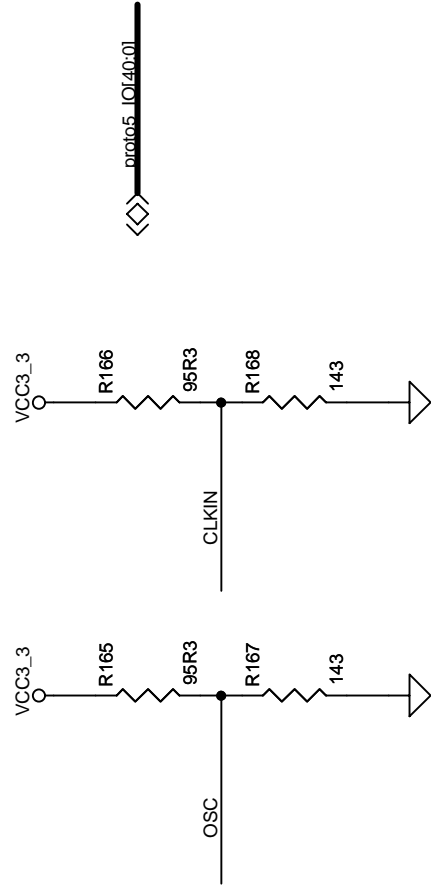
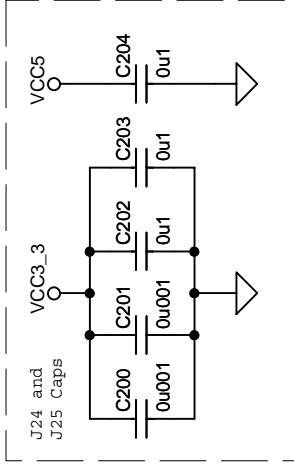
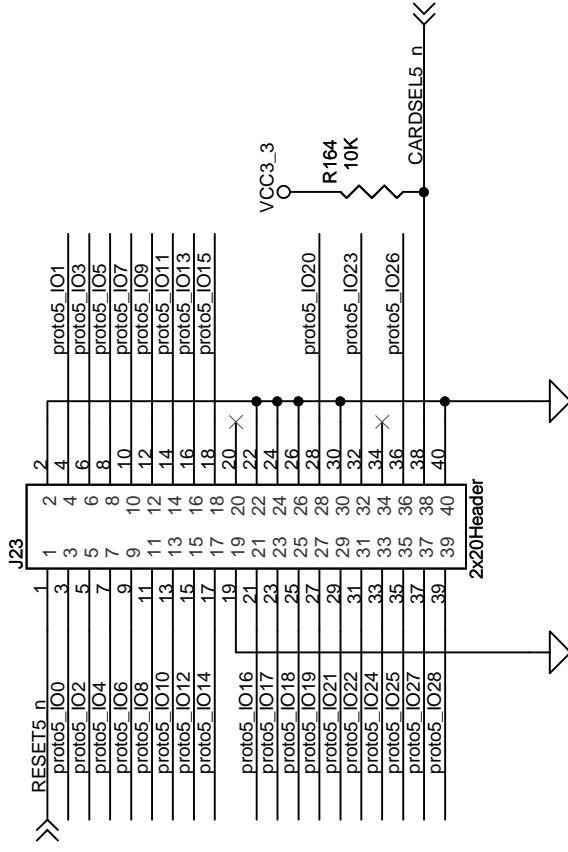
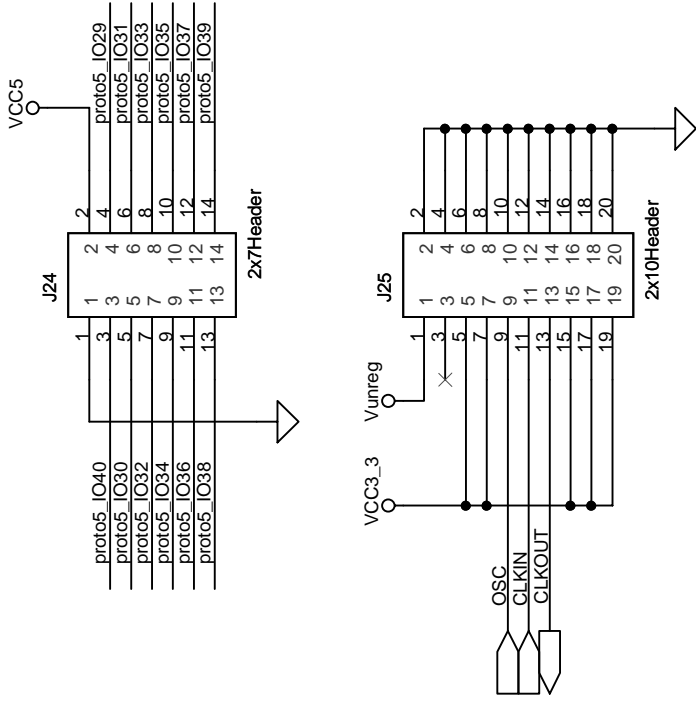
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# Protocard 1



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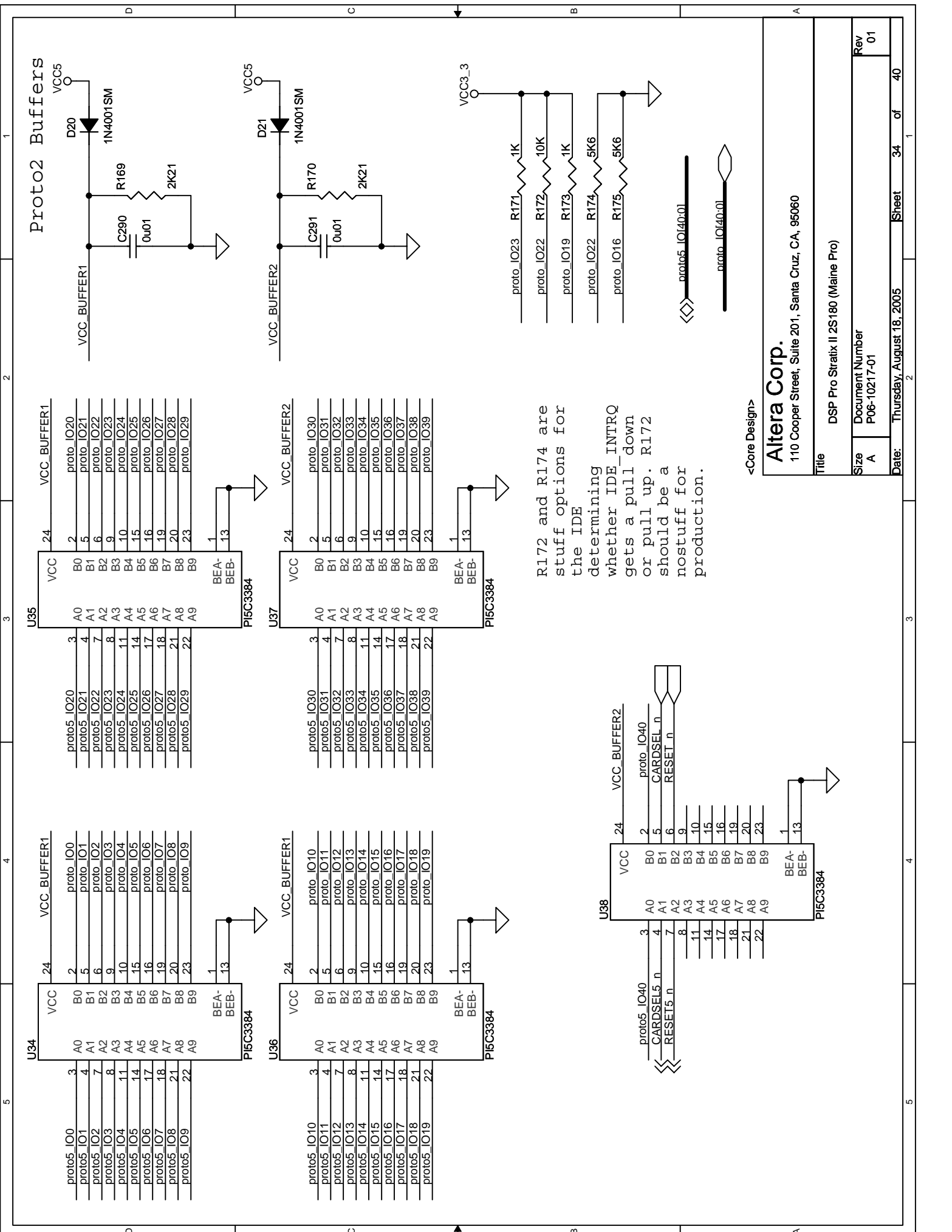
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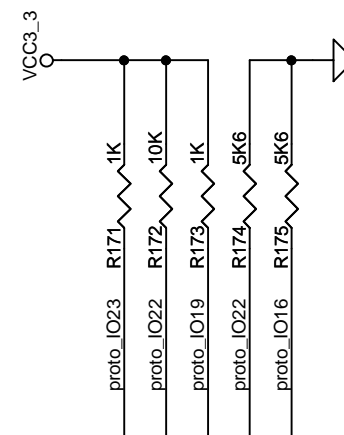
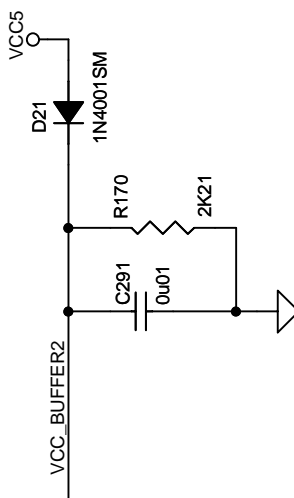
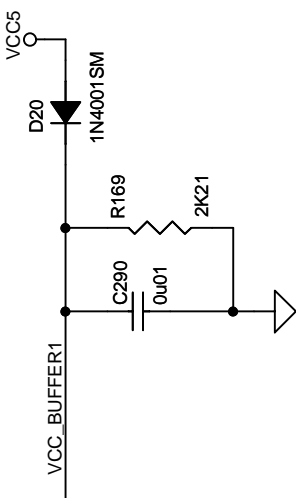
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**Proto2 Buffers**



R172 and R174 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.

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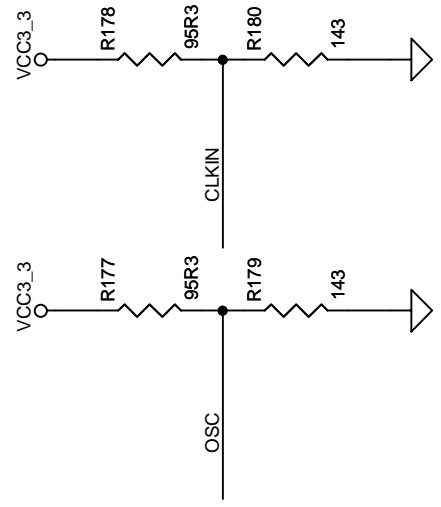
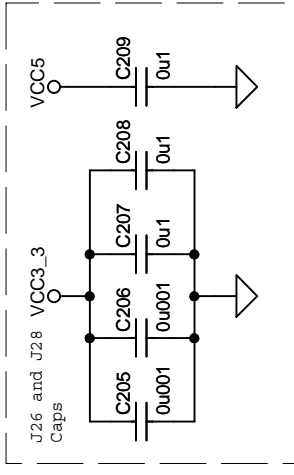
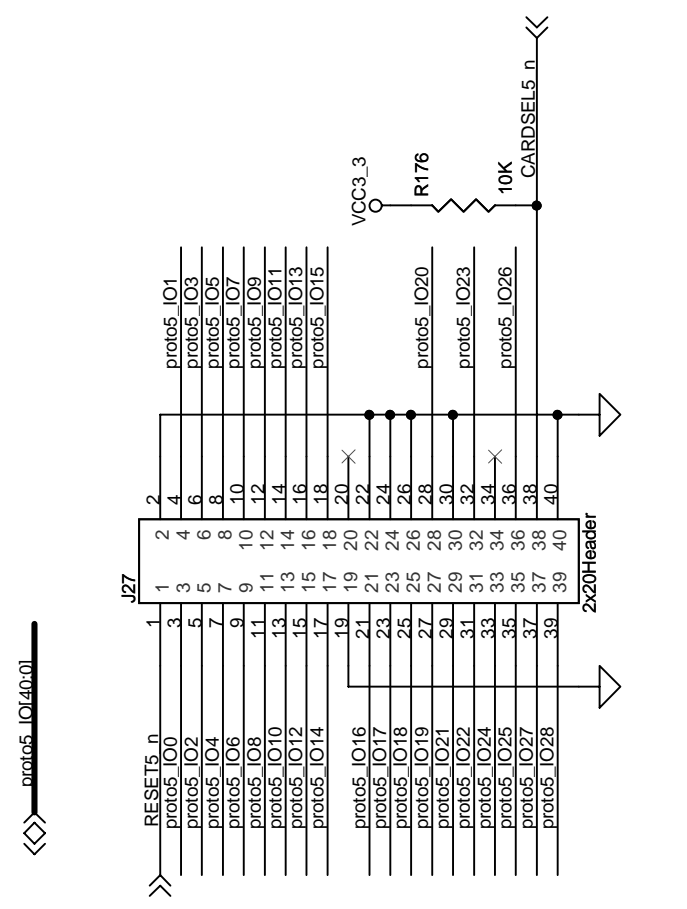
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1 2 3 4 5

D C B A

# Proto2 Headers



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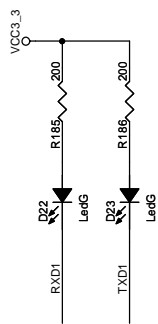
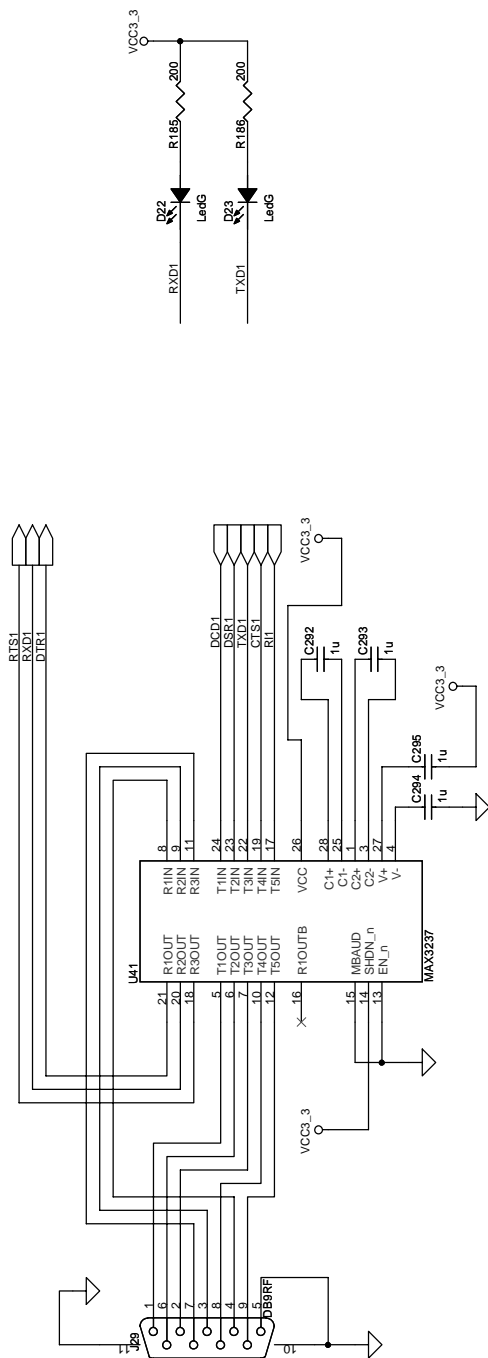
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Serial Ports



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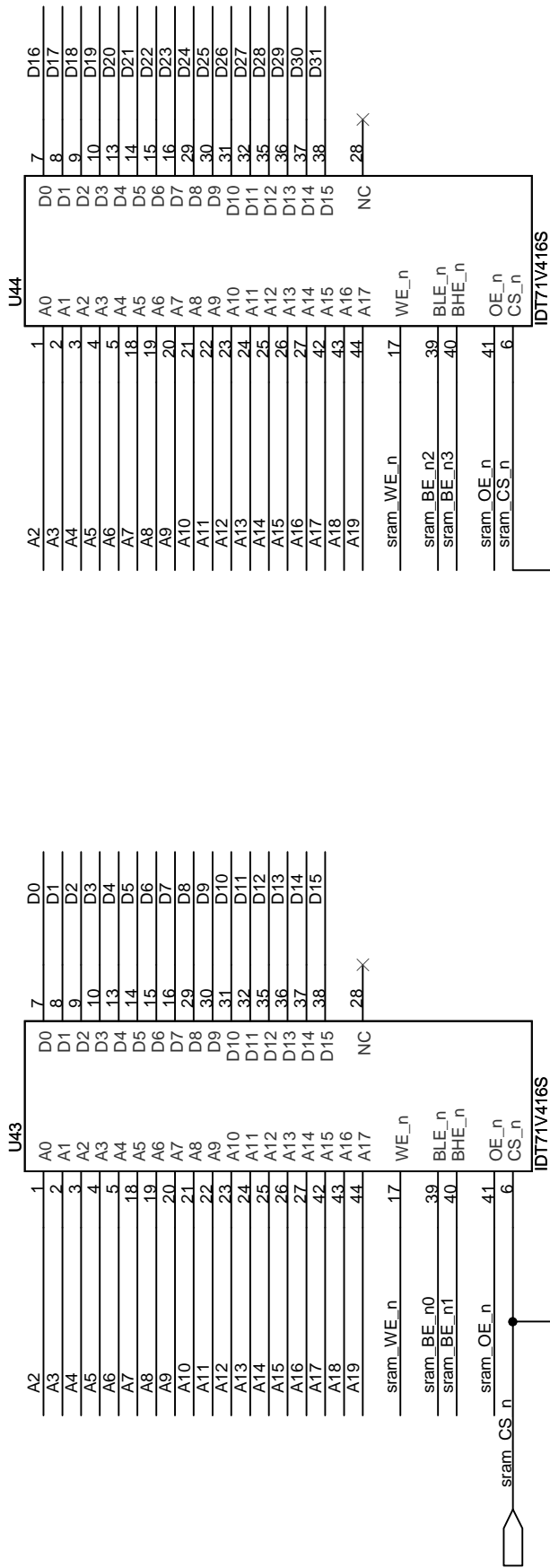
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Size B Document Number P06-10217-01

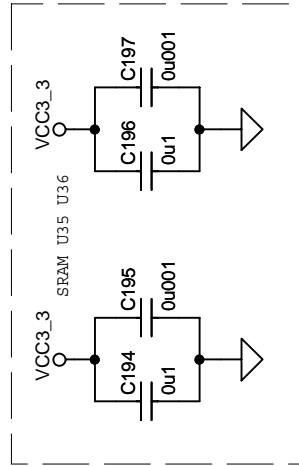
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SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM  
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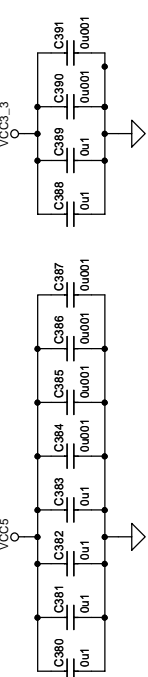
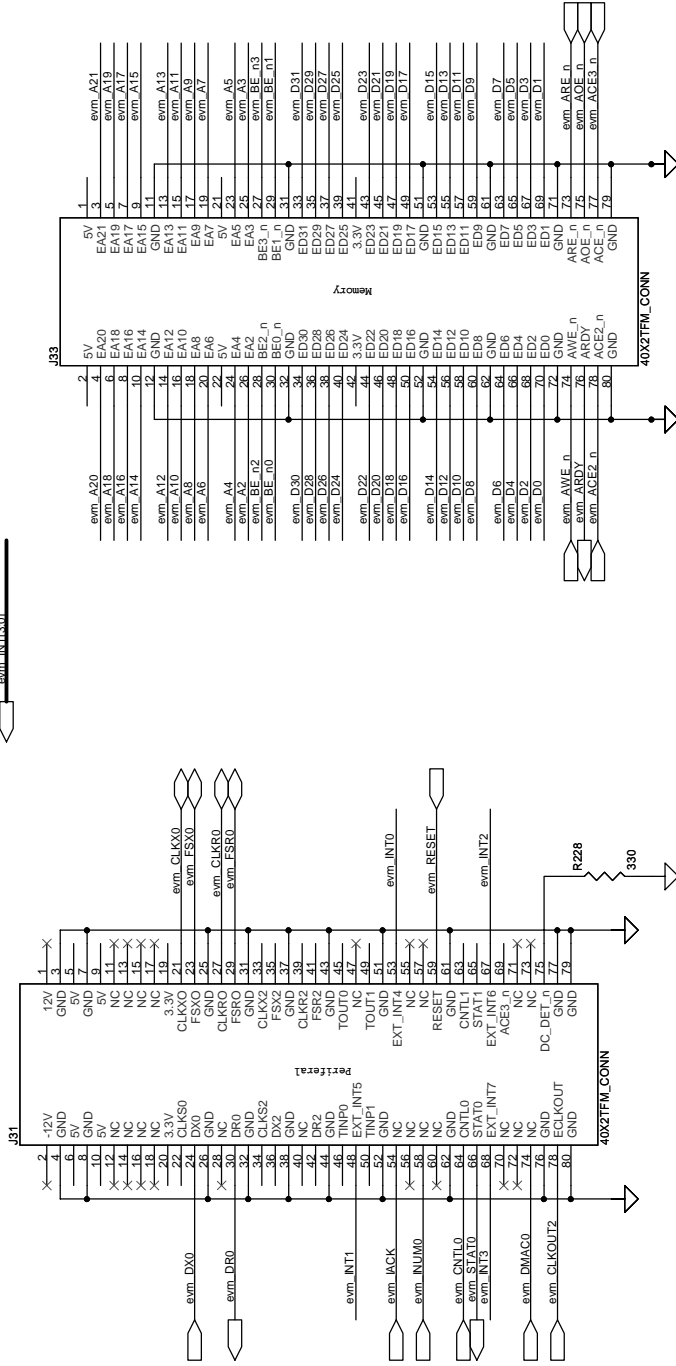
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3.00" apart

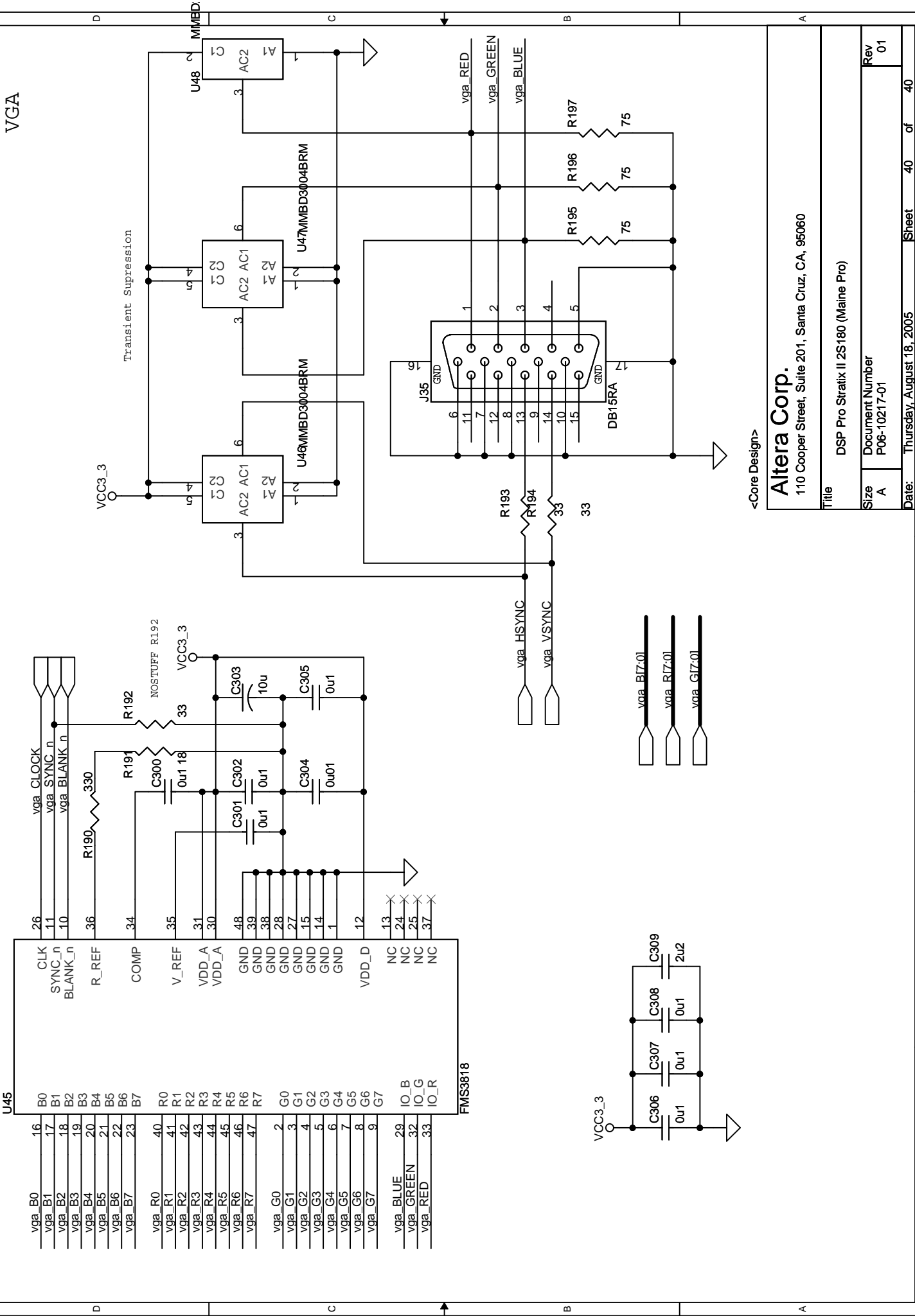


These connectors reference the TI 6416 board

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VGA



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vga_B0	16	CLK	26
vga_B1	17	SYNC_n	11
vga_B2	18	BLANK_n	10
vga_B3	19		
vga_B4	20	R_REF	36
vga_B5	21	COMP	34
vga_B6	22	V_REF	35
vga_B7	23	VDD_A	31
		VDD_A	30
vga_R0	40	GND	48
vga_R1	41	GND	39
vga_R2	42	GND	38
vga_R3	43	GND	28
vga_R4	44	GND	27
vga_R5	45	GND	15
vga_R6	46	GND	14
vga_R7	47	GND	1
vga_G0	2	VDD_D	12
vga_G1	3	NC	13
vga_G2	4	NC	24
vga_G3	5	NC	25
vga_G4	6	NC	37
vga_G5	7		
vga_G6	8		
vga_G7	9		
vga_BLUE	29		
vga_GREEN	32		
vga_RED	33		

FMS3818